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Energy-Efficient SAR-ADC Architecture for 6G - Applications

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Abstract:- As high-speed wireless communication and sensing technologies advance in the D-band (110–170 GHz), there is an increasing demand for efficient, low-power digital-to-analog (DAC) and analog-to-digital converters (ADC). This paper introduces an innovative multiplexed R-2R DAC paired with a successive approximation register (SAR) ADC, designed specifically to optimize performance in high-frequency D-band applications. The proposed architecture leverages the efficiency of the R-2R ladder to achieve low-power operation while ensuring high linearity. Additionally, multiplexing enhances throughput without significantly increasing power consumption. The SAR ADC is optimized for energy-efficient high-speed conversion, making it suitable for power-constrained mm Wave systems. The design is implemented in a 180nmCMOS-based technology process in cadence design suite and demonstrates superior power efficiency, compact area utilization, and high signal integrity, making it a viable solution for next-generation high-frequency applications such as 6G communication, radar, and high-resolution imaging.

Keywords*: DAC, SAR ADC, R-2R DAC, Analog-to-Digital Conversion, D-band applications, Cadence Design Suite, 6G applications.*

1. Introduction

With the rise of high-frequency wireless technologies like 6G communication and radar imaging, there is a growing demand for advanced digital-to-analog and analog-to-digital converters. The D-band (110–170 GHz) stands out as a crucial frequency range for next-generation applications, offering the potential for ultra-high data rates and enhanced spatial resolution. However, designing efficient and power-conscious mixed-signal circuits for this frequency range presents significant challenges.

Traditional DAC architectures, like current-steering designs, tend to consume significant power and pose layout challenges at extremely high frequencies. In contrast, the R-2R ladder DAC offers a more efficient solution, leveraging its straightforward resistor-based structure. Additionally, incorporating a multiplexing technique boosts the effective sampling rate without a proportional rise in power consumption, making it well-suited for high-speed applications.

SAR ADCs are known for their energy efficiency, making them an ideal choice for integration with low-power DAC architectures. By fine-tuning the SAR ADC for high-speed performance, we strike a balance between power efficiency and conversion speed. This seamless integration supports effective digital-to-analog and analog-to-digital conversion in mmWave systems while ensuring minimal power consumption and compact design.

This paper presents the design, implementation, and performance analysis of a low-power multiplexed R-2R DAC coupled with a SAR ADC for D-band applications. The proposed system is implemented in a CMOS-based process and evaluated for power efficiency, linearity, and high-frequency performance. The results demonstrate the feasibility of our approach in advancing next-generation wireless and sensing technologies.

2. Related Works

[1] The development of SAR ADCs has been driven by the need for energy-efficient and high-performance solutions across various applications. Analyzing both established methods and recent innovations provides key insights into optimizing SAR ADC architectures. In 2016, researchers proposed a framework for SAR ADC design focused on asynchronous architectures. They introduced a hybrid sizing methodology that integrates

knowledge-based and optimization-driven approaches to enhance tool efficiency and streamline the design process. This method reduces complexity, improves reliability, and enables asynchronous SAR ADCs to achieve superior power efficiency and speed compared to synchronous designs. Their approach balanced automation with expert intuition, laying the groundwork for future advancements in ADC technology.[2] Expanding on this foundation, Tang et al. (2022) investigated advanced methodologies to improve the energy efficiency of SAR ADCs, pushing the boundaries of low-power design while enhancing overall performance. *They addressed core component optimizations, including comparators, capacitive DACs, and SAR logic. Innovations such as enhanced DAC switching schemes and advanced comparator structures minimized power consumption and improved accuracy. By leveraging modern CMOS technologies, these techniques mitigated dynamic noise and other non-idealities, bridging the gap between high-level design methodologies and practical component-level enhancements.*

[3] Expanding Design Paradigms with Pipelined ADCs. Mirzaie and Byun (2018) explored pipelined ADC architectures to address the needs of high-speed, high-resolution applications. Their work employed a multi-objective evolutionary algorithm to optimize performance and yield under process variations. This approach uses Pareto-optimal trade-offs and achieves good results, including a value of 121 fJ/level of change (FoM). Combining research with optimization, this work demonstrates that there are many aspects of ADC design in different dimensions. Modularization, also proposed by Huang et al., is implemented through behaviour and look-up tables (LUTs). This approach maximizes the efficiency of SAR ADC architectures and accounts for drawbacks such as clock jitter, device mismatch, and noise. The proposed design demonstrates robustness in managing process-level changes, as exemplified by its implementation in a 14-bit, 4.2 MSPS SAR ADC. This approach is compatible with the process and optimization process, simplifies the design cycle, and increases reliability. Gaining a deep understanding of electrical engineering lays the groundwork for exploring and incorporating these technologies into SAR ADC development.

[4] To tackle the challenges of rising power consumption, input capacitance, and chip area at higher resolutions, Lin et al. proposed an all-digital time-domain delay interpolation technique. This approach utilizes delay interpolation between adjacent comparators to generate additional quantization levels, enhancing resolution while minimizing power and latency impact.

3. Proposed System

The proposed architecture combines a low-power multiplexed R-2R DAC with a SAR ADC tailored for D-band applications. It is engineered to ensure high linearity, minimal power consumption, and efficient area utilization while sustaining high-speed performance. The primary components of this system include:

1. Input Op-Amp:

The SAR ADC begins with a high-speed operational amplifier, which compares the input analog voltage (Vin) to the feedback voltage from the DAC. If Vin exceeds the DAC-generated voltage, the SAR logic assigns a '1' to the corresponding bit; otherwise, it assigns a '0' [5].

2. Successive Approximation Register (SAR):

This digital control block generates an 8-bit digital output by performing a binary search on the input voltage. It successively updates the DACs to find the closest approximation of **Vin**.

3. Multiplexed R-2R DAC:

Multiplexed DAC (DAC1 & DAC2): The DACs convert digital bits back into an analog voltage for comparison. DAC1 processes the lower bits (b0–b3), and DAC2 processes the higher bits (b4–b7). The multiplexing approach helps in optimizing speed and reducing power consumption.

4.Implementation in Cadence:

The entire system is designed and simulated using the Cadence Virtuoso toolset. Layout optimizations, parasitic extraction, and post-layout simulations are performed for further improvement [6].

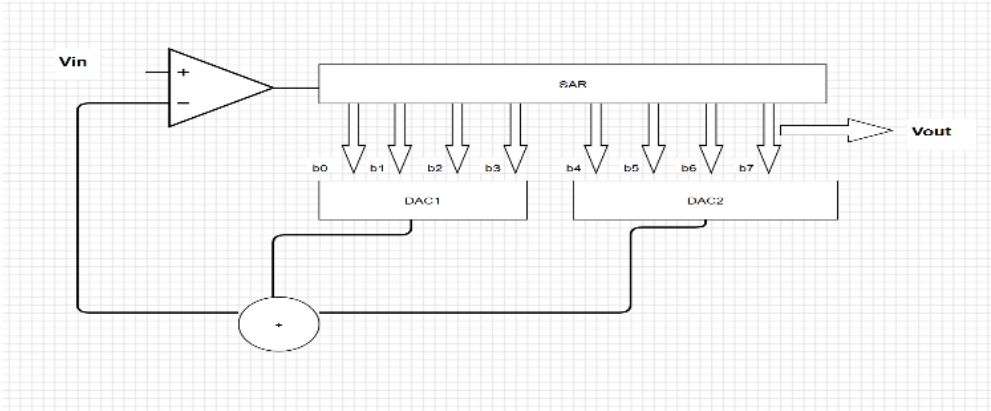

Figure 1: SAR-ADC Circuit Diagram

The simplified design incorporates multiplexers within the circuit, streamlining its structure and minimizing the complexity and risks associated with DAC design.

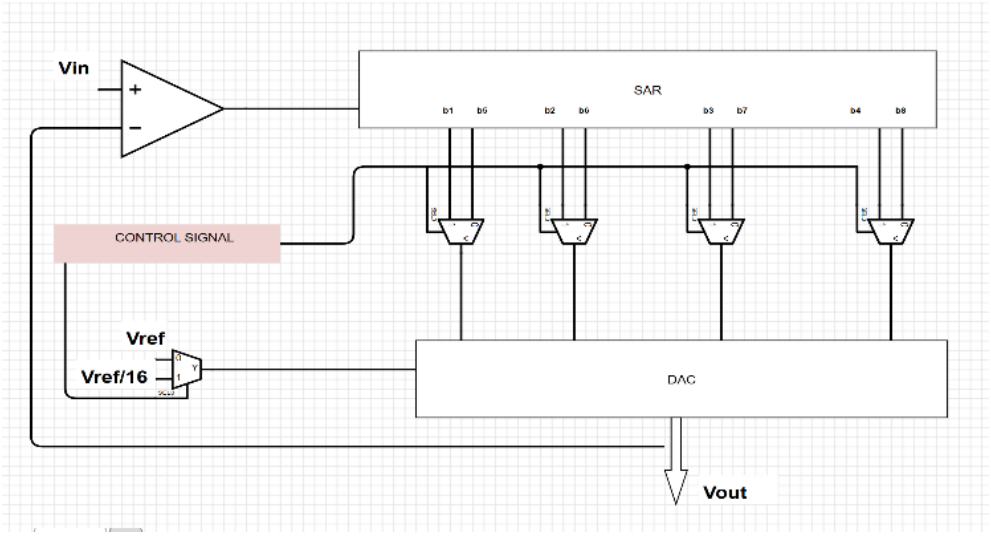

Figure 2: Multiplexed R-2R DAC

In this paper our aim is to design the R-2R DAC in different simplified ways to finally implement a low power, high speed and high-resolution SAR-ADC for applications such as 6G communication. Figure 2. Will be further modified as below by having 4-bit SAR with both LSB and MSB bits.

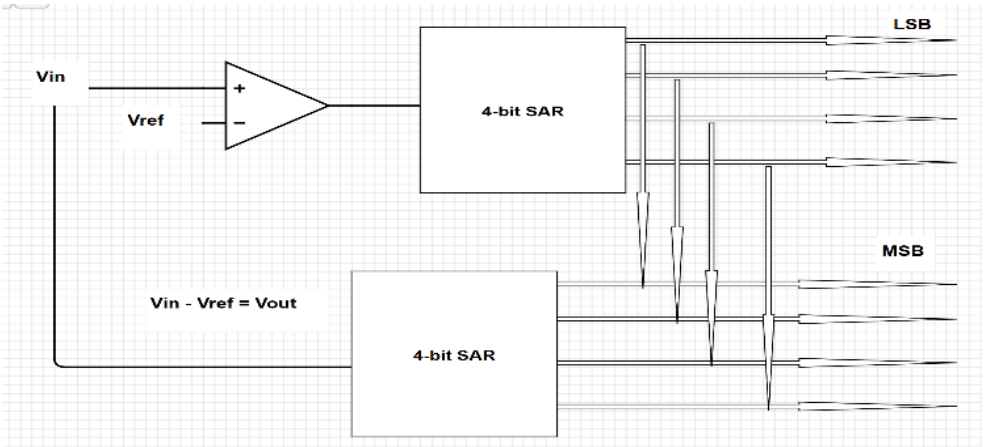

Figure 3: Simplified SAR-ADC

A. Design and Sub Circuits

This design is tailored for low-power, high-speed performance, making it ideal for D-band (110-170 GHz) applications. It comprises multiple subcircuits that collaborate to enable efficient digital-to-analog and analog-to-digital conversion at mmWave frequencies.

Operational Amplifier

The operational amplifier serves as a key component in the SAR ADC architecture, ensuring feedback loop stability and enabling precise voltage control. It is designed with the combination both differential amplifier and common source amplifier. Op-Amp design using a combination of Common Source and Differential Amplifiers is an excellent choice for the SAR ADC system [7]. It provides high gain, wide bandwidth, low noise, and low power consumption, making it ideal for high-speed DAC applications in the D-band frequency range. So that it has better Common-Mode Rejection Ratio (CMRR) (60-80dB) and power efficiency.

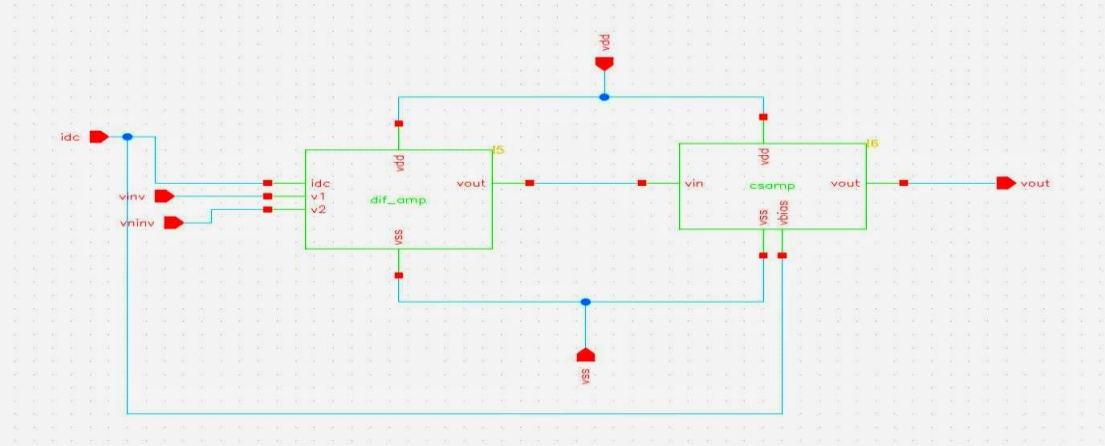

Figure 4. Operational Amplifier Schematic

R2R DAC

The R-2R DAC is designed to provide the accurate, efficient digital-to-analog conversion required for the bit estimation process of SAR ADCs. It provides linearity and reduces speed change time by matching resistance[8]. The design focuses on reducing negative factors such as glitches and parasitic capacitance to improve overall performance. Simulation and layout optimization ensure that the DAC meets the resolution and power requirements of the ADC, providing a reliable foundation for high-performance, low-power applications.

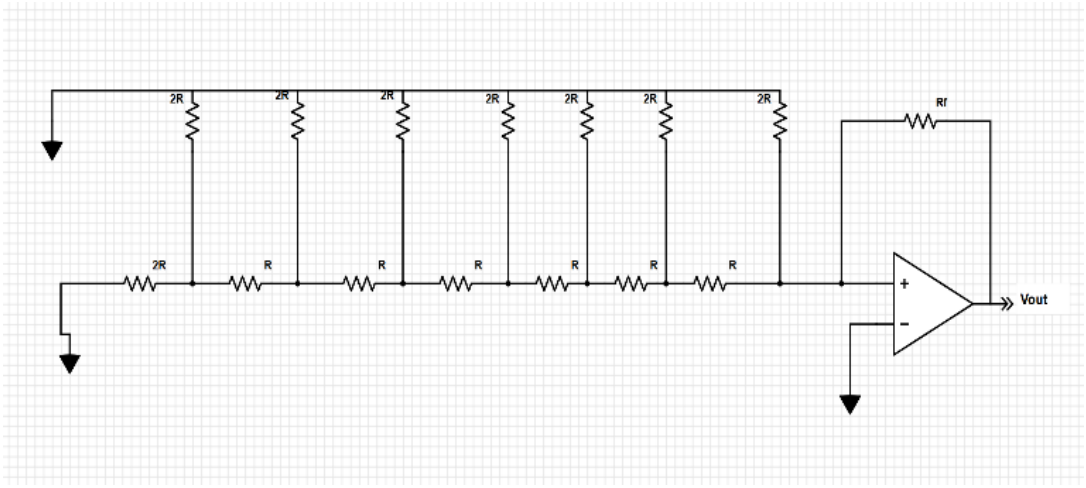

Figure 5: R2R DAC Schematic

B. System Integration

Vin (Analog Input): The Sample-and-Hold (S/H) circuit captures and stabilizes the input signal.

S/H Output: The comparator evaluates the input voltage against the DAC output.

Comparator Result: The output is sent to the SAR logic, which updates the DAC accordingly.SAR Output (Digital Bits): Drives the multiplexed R-2R DAC.

DAC Output (Analog): Reused by Comparator for next iteration.

Final SAR Output (8-bit Digital Code): Output to digital system.

Equations:

$$V\_out = V\_ref * (b1 * 2^{-1} + b2 * 2^{-2} + + b3 * 2^{-3} + + \ldots + b8 * 2^{-4}) \quad (1)$$

$$V\_out = Vref * (b1 * 2^{-1} + + b2 * 2^{-2} + + b3 * 2^{-3} + + b4 * 2^{-4}) \quad (2)$$

$$V\_out = Vref/2^{4} * (b5 * 2^{-1} + + b6 * 2^{-2} + + b7 * 2^{-3} + + b8 * 2^{-4}) \quad (3)$$

C. Methodology

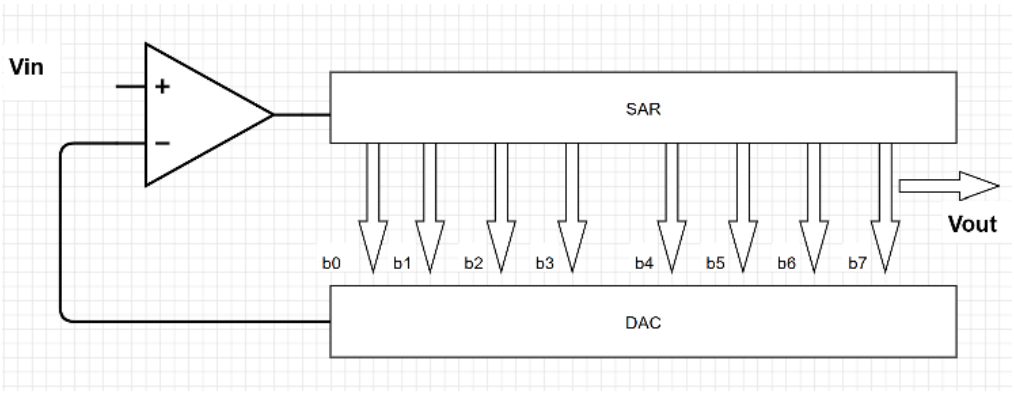

Figure 6: SAR ADC Methodology

Operational Amplifier (Op-Amp): The operational amplifier is a core component in the SAR ADC, responsible for precise voltage comparison during the successive approximation process. The design of the op-amp focuses on achieving low offset voltage, high-speed operation, and low distortion[9]. These characteristics are necessary for accurate bit-by-bit conversion and minimizing errors during the SAR cycle.

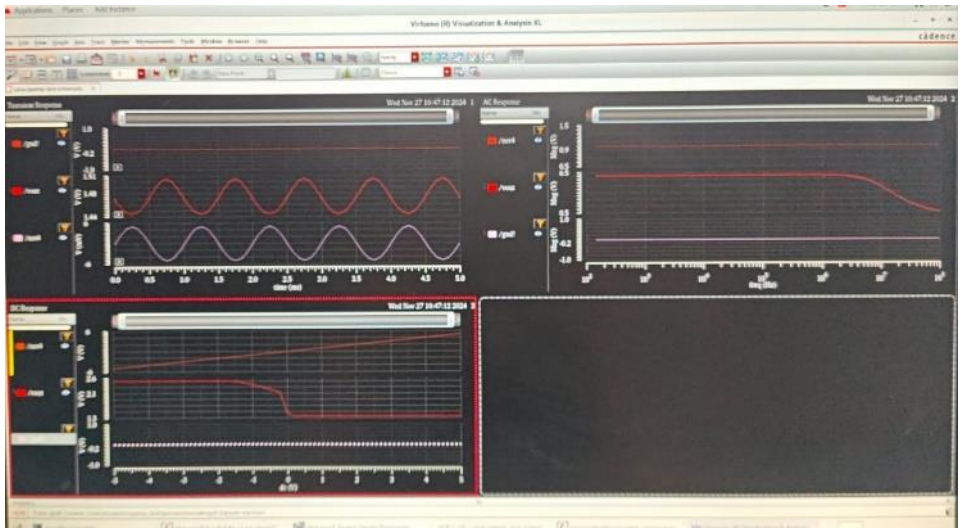

Figure 7: Operational amplifier output waveforms

R-2R DAC (Digital-to-Analog Converter): The R-2R DAC is an essential component of the SAR ADC, providing a precise reference voltage for comparing the input signal.It utilizes a resistor ladder network with R and 2R values to establish precise voltage levels. The design prioritizes minimizing switching errors and capacitive loading while ensuring fast switching times for accurate and efficient voltage step generation[10].

Figure 8: R2R DAC Output Waveforms

4. Results and Discussion

Performance Evaluation of the 20 GSps SAR ADC, incorporating a multiplexed R-2R DAC, was designed and simulated in Cadence to achieve ultra-high-speed performance for D-band (110–170 GHz) applications. The primary objective was to achieve a sampling rate of 20 GSps, ensuring high-speed data conversion with minimal power consumption.

5. Conclusion

A conventional SAR ADC utilizing an R-2R DAC in the feedback loop experiences conversion delays. To enhance processing efficiency, this design implements an 8-bit R-2R DAC by integrating two 4-bit DACs, each operating with distinct reference voltages. Since conversion happens in one clock-cycle so low power and high-speed metrics are met. Further the input voltage is subtracted from reference voltage and two low power SAR are used to obtain LSB and MSB bits. These ADC which is developed are suitable for 6G communications.

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