

Design and study low power consumption high speed CMOS Push – Pull Amplifier

Arvind Tiwari & K.K. Shukla

Department of Physics, Maharishi University of Information Technology, Lucknow U.P. India

Abstract- In this paper author's present novel model of push pull amplifier circuits with proper of alongside element like capacitor. In this paper use of addition element make circuit **flexible** and **versatile** therefor proposed circuit can be used from narrow band to wideband amplifier. Proposed circuit shows best temperature stability in the range between -20°C to 80°C . Proposed circuit simulated using MATLAB and cadence virtuoso software and study about frequency response, temperature stability, current gain, voltages gain with variations of used additional circuit 1pF to 10F.

Key Words: -CMOS push pull amplifier, High speed, low power, voltage gain, wideband

Introductions-

When reviewing the available literature from various sources such as internet databases, IEEE journals, research papers, and theses, we found extensive work on different types of transistor amplifiers designed for specific purposes. One widely used configuration is the NPNtransistor Darlington pair amplifier [1,2,3], a popular circuit consisting of cascaded emitter followers. The primary advantage of this configuration is its ability to increase input impedance while reducing output impedance. However, its main drawback is that its voltage gain is nearly equal to one [4,5]. Another known design is the Sziklaipair amplifier [6,7], also called the feedback pair amplifier, which offers improved linearity and bandwidth compared to the Darlington pair. RC coupledamplifiers [8], or resistance-capacitance transistor amplifiers, face the disadvantage of poor impedance matching. Other types of amplifiers, such as transformer-coupled and transistor push-pull amplifiers, have been shown to perform well within the audio frequency range, but the main issue with these systems is power loss due to heat generation.

Recent research has increasingly focused on CMOS technology [9,10] (Complementary Metal-Oxide-Semiconductor), which is built using N-channel and P-channel MOSFETs [11]. The key advantage of CMOS lies in its flexible device behavior. In this work, we focus on using CMOS technology to design a novel circuit for multipurpose applications by incorporating a variety of additional circuit elements such as capacitors [12,13,14].The proposed circuit performs better than amplifiers based on the Sziklai and Darlington pairs, as these amplifiers function well in the audio frequency range (1 Hz to 20 kHz) but do not respond as effectively at higher frequencies [15,16]. In contrast, CMOS-based circuits provide superior performance across both the audio and radio frequency ranges. Therefore, we propose replacing the Darlington and Sziklai pairs in conventional circuits with CMOS technology in a quasi-complementary Class B push-pull amplifier, which demonstrates high efficiency and better linearity at high frequencies.

The primary advantages of CMOS-based devices include very low power consumption and excellent noise immunity, meaning they generate minimal heat. All simulations in this work were conducted using **MATLAB** and **Cadence Virtuoso 180nm technology**.

Experimental Circuits- In these sections we present circuit elements detailed of reference and proposed circuit.

S.N.	Circuit Elements	Reference circuit	Proposed circuit
1	Input voltage	15 μ Vac & 0 Vdc	15 μ Vac& 0 Vdc
2	Cin	10 μ F	10nF
3	Rin	10K Ω	1 Ω

4	D2,D2,D8,D9	DIN4002	-
5	R1R2R11R12	10K Ω	1K Ω
6	V1&V2	20Vdc	20Vdc
7	NMOS	IRF9140	-
8	PMOS	IRF150	

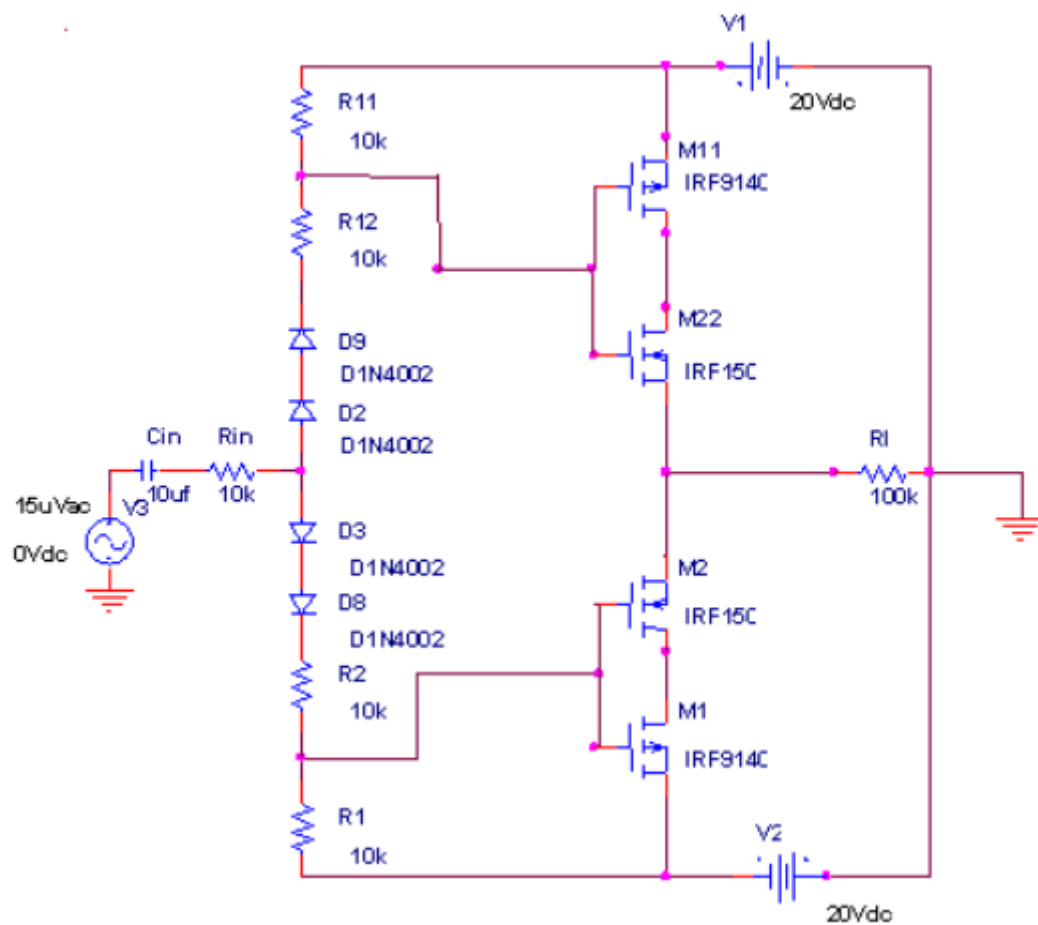


Fig.1 Reference circuit of CMOS push pull amplifier [17]

Reference push pull amplifier circuits shown in figure 1 [17]. And the proposed CMOS amplifier circuits presented in figure 2. In proposed circuit additional circuit elements capacitor connected I series with Dc power supply and all diode replace with resistance with 1K Ω and remaining elements are same as reference circuit.

✓

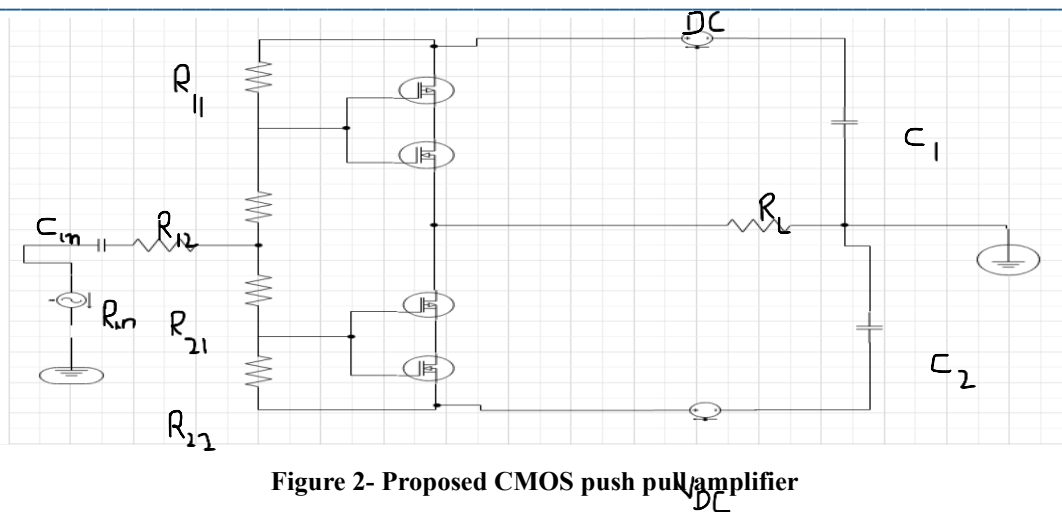


Figure 2- Proposed CMOS push pull amplifier

Result and Discussions- In this section firstly we analysed frequency response with variations of additional circuit elements capacitor from nano Fared to farad it is found that proposed CMOS push pull amplifier effectively work audio to radio frequency range i.e. 20Hz to 1THz. It is simulated by two methods one Cadence Virtuoso and other is MATLAB. The frequency response curve orange line shows MATLAB simulated curve and black line curve shows cadence virtuoso curve shown in figure 3, and comparison of bandwidth between reference and proposed circuit in at variations of capacitor are presented in table 1.

S.N.	Capacitor value	Reference bandwidth	Proposed bandwidth by cadence	Proposed bandwidth by MATLAB
1	1nF	-	23.6 KHz	25.3 KHz
2	1uF	12.3 KHz	1.23 MHz	1.35 MHz
3	1mF	2.35MHz	63.5MHz	70.7 MHz
4	1F	6.3GHz	23.9GHz	25.6 GHz
5	10F	63.5GHz	0.15THz	0.25 THz

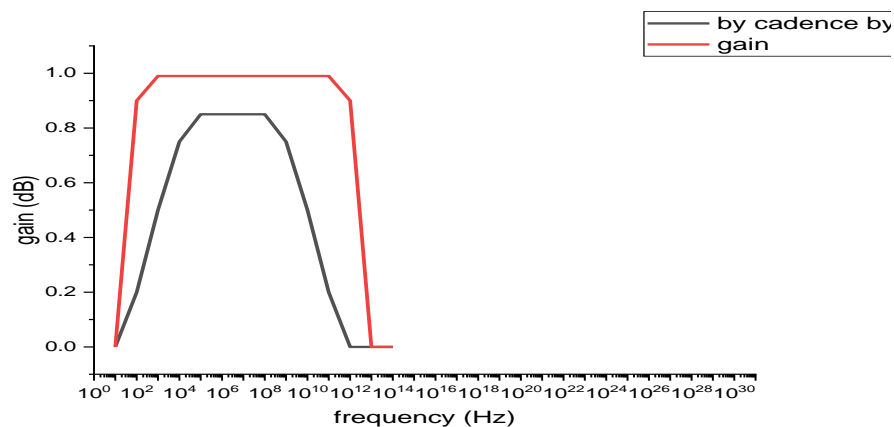


Figure 3- frequency response curve of proposed circuit at the value of additional elements 1F.

Now we have discuss temperature stability with frequency response, and it found that proposed circuit shows excellent temperature stability between the range of temperature -20°C to 80°C . this study done by using both simulation software Cadence virtuoso and MATLAB. Figure 4 represent temperature stability graph, in this graph orange line shows MATLAB curve and black line represent cadence virtuoso study.

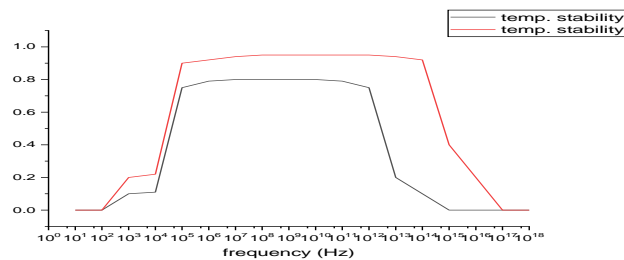


Figure 4- temperature stability between -20°C to 60°C of proposed circuit in frequency response curve.

In this part we study input impedance using simulation tool both simulations software cadence and MATLAB. Figure 5 represent input impedance of proposed CMOS push-pull amplifier. In figure 5 orange line represent MATLAB study and black line represent cadence study.

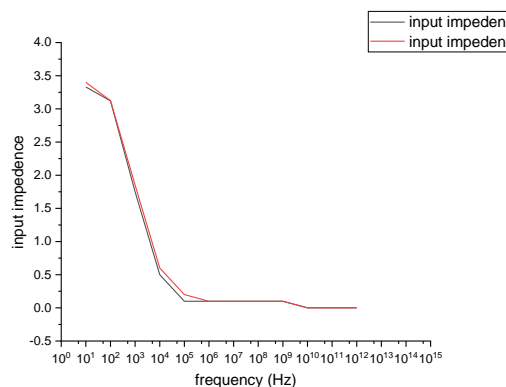


Figure-5 Input impedance of proposed CMOS push pull amplifier.

Figure 6 represent transient analysis of CMOS push pull amplifier at 1GHz input frequency.

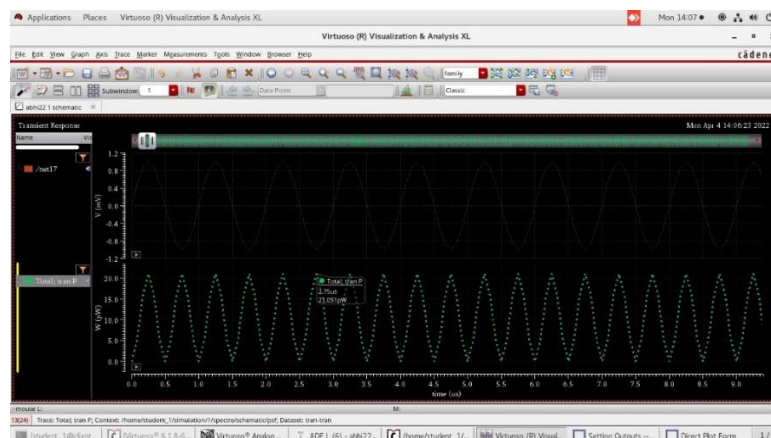


Figure 6 Transient analysis of CMOS push pull amplifier

Finally, we focus most important parameter output noise and it found that output noise is very low. Figure 8 shows output noise of proposed push pull amplifier.

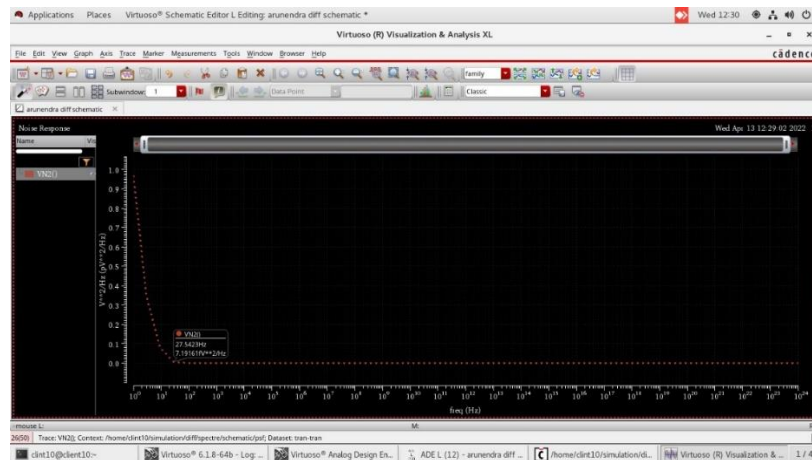


Figure- 8 Output noise of proposed push pull amplifiers.

Now we study voltage gain with frequency for different value of addition circuit elements, in table 2 represent variation of voltage gain with frequency at various value of capacitor from 1nF to 10F.

S.N.	Values of capacitors	Voltage Gain at 10KHz		Voltage Gain at 1GHz		Voltage Gain at 1THz	
		Reference	Proposed	Reference	Proposed	Reference	Proposed
1	10nF	287.69	356.39	5.3102	153.63	543.192	654.98
2	10μF	44.75	109.63	10.246	89.632	112.957	210.632
3	1mF	44.562	110.24	12.36	75.253	112.556	202.637
4	10F	295.521	342.352	858.36	996.563	537.502	756.693

In the section we present circuit layout designed using MATLAB, figure 9 represent layout of proposed push pull amplifier circuit.

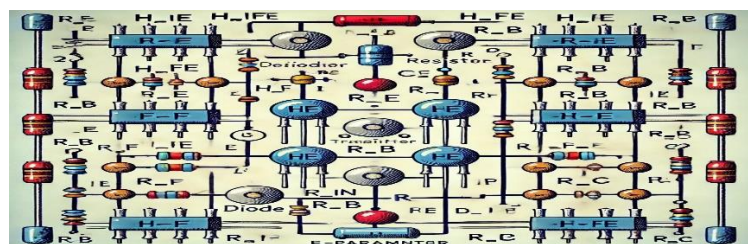


Figure 9 proposed circuit layout

So, the most important outcome of this study is proposed circuit very effective in THz region.

Conclusion- Based on the simulation study, it was observed that the careful selection of additional circuit elements plays a crucial role in making the proposed CMOS amplifier flexible and versatile. As a result, the circuit is capable of operating across various frequency ranges, from tuned narrow-band to wide-band amplification. The output noise is minimal, while both voltage gain and current are high, and the amplifier operates at high speed. Therefore, the proposed amplifier can function effectively as a high-speed operational amplifier.

Reference's-

- [1] Arshad, Syed Shamroz, Geetika Srivastava, and SachchidaNand Shukla. "Design of ultra-wideband Sziklai pair based LNAs for wireless communication applications." *International Journal of Information Technology* (2024): 1-19.
- [2] Singh, Rashmi, and Rajesh Mehra. "Analysis of Darlington pair amplifier at 90nm technology." In *2016 International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT)*, pp. 3637-3641. IEEE, 2016.
- [3] Singh, Sanyokita, B. B. Soni, and Puran Gour. "High Quality Factor Two Notch Low Noise Darlington Amplifier for Low Frequency Application." In *2015 International Conference on Computer Communication and Informatics (ICCCI)*, pp. 1-5. IEEE, 2015.
- [4] Arshad, Syed Shamroz, SachchidaNand Shukla, Aditya Kumar Sharma, and Geetika Srivastava. "Darlington pair based Small-Signal amplifier under triple transistor topology." *Journal of International Academy of Physical Sciences* 26, no. 4 (2022): 427-442.
- [5] Shukla, SachchidaNand, and Beena Pandey. "Two-stage small-signal amplifier with Darlington and Sziklai pairs." In *2014 IEEE International Conference on Semiconductor Electronics (ICSE2014)*, pp. 13-16. IEEE, 2014.
- [6] Shukla, Sachchida Nand, Pratima Soni, Naresh Kumar Chaudhary, and Geetika Srivastava. "Development of low frequency small signal amplifier using BJT-JFET in sziklai pair topology." *International Journal of Recent Technology and Engineering* 9, no. 3 (2020): 217-223.
- [7] Shukla, SachchidaNand. "New small-signal amplifying system with Sziklai pairs in triple-transistor topology." In *2016 International Conference on Advances in Electrical, Electronic and Systems Engineering (ICAEEES)*, pp. 463-468. IEEE, 2016.
- [8] Higashimura, M., and Y. Fukui. "RC active realization of mutually coupled circuit." In *1991., IEEE International Symposium on Circuits and Systems*, pp. 1343-1346. IEEE, 1991.
- [9] Tiwari, Raj Kumar, and Gaya Prasad. "CMOS Compound Pair Wide Band Bio-Amplifier." *Editorial Committees* (2014).
- [10] Tiwari, Raj Kumar, Ganga Ram Mishra, and Maheshwar Misra. "A new high performance CMOS differential amplifier." *International Journal of Electronic Engineering Research, ISSN* (2009): 0975-6450.
- [11] Chen, Xinghao, and Nur A. Toubia. "Fundamentals of CMOS design." In *Electronic Design Automation*, pp. 39-95. Morgan Kaufmann, 2009.
- [12] Zhang, Qingzhu, Yongkui Zhang, Yanna Luo, and Huaxiang Yin. "New structure transistors for advanced technology node CMOS ICs." *National Science Review* 11, no. 3 (2024): nwae008.
- [13] Ahmed, Rekib Uddin, Harsh Raj Thakur, M. A. Seenivasan, and Prabir Saha. "Power-efficient VLSI realization of decimal convolution algorithms for resource-constrained environments: a design perspective in CMOS and double-gate CMOS technology." *Microsystem Technologies* (2024): 1-13.
- [14] Bhuiyan, Mohammad Arif Sobhan, Md Rownak Hossain, Mohammad Shahriar Khan Hemel, Mamun Bin Ibne Reaz, KhairunNisa'Minhad, Tan Jian Ding, and Mahdi H. Miraz. "CMOS low noise amplifier design trends towards millimeter-wave IoT sensors." *Ain Shams Engineering Journal* 15, no. 2 (2024): 102368.
- [15] Sharroush, Sherif M., and Yasser S. Abdalla. "Two proposed BiCMOS inverters with enhanced performance." *Ain Shams Engineering Journal* 15, no. 1 (2024): 102259.
- [16] Cui, Chuanjie. "Analysing CMOS performance: A comprehensive study of operational characteristics in low-temperature environments." In *Journal of Physics: Conference Series*, vol. 2786, no. 1, p. 012009. IOP Publishing, 2024.
- [17] Tiwari, Monika, G. R. Mishra, and Vineet Tiwari. "A New Circuit Model for Low Voltage High Speed CMOS Push-Pull Amplifier."