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A Novel Hybrid High Level MLI Topology for Industrial and Agricultural Applications

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Abstract:

The Renewable Energy Sources (RES) are the primary source of energy because of reduction in fossil fuels day to day. The primary resource in all available non-conventional energy sources is solar energy. Solar energy is obtained normally from Photo Voltaic (PV) cells. In PV cells a photo diode is used which converts the sun irradiation into DC voltage, which is normally a low value, so this is not sufficient to run the electrical loads which are connected to the micro grids. To avoid this problem, a novel boost converter is needed to improve the voltage profile, but it has a problem of high ripple content in voltage profile, which is not preferable for giving as i/p to the Inverter. Normally inverter will take constant DC as an i/p and convert into Alternating Current (AC) voltage. To avoid the above-described ripple, connect problem of boost converter, a novel hybrid Pulse Width Modulation (PWM) DC -DC converter is presented in this paper along with a SPWM inverter circuit which finds its applications in micro grids. The topology of 31-level inverter has been analyzed with reduced number of switches also discussed in this paper. In traditional topologies a greater number of switches are required, and it can be decreased by planning the diverse topologies. The current distinctive topology is described and compared with the conventional configurations and the corresponding results are presented. With this it can be observed that the proposed topology gives the better outcomes. This can be utilized as a part of various micro grid inverter applications.

Keywords-Renewable Energy Sources (RES),Photo Voltaic (PV), Total Harmonic Distortion (THD),Pulse Width Modulation (PWM), Cascaded H-Bridge (CHB),Input(i/p), Output(o/p).

I. Introduction:

In current days, main role in power generation is with Renewable Energy Sources (RES) because of reduction in the fossil fuels normally acts as the main component of all readily available non-conventional energy sources. Energy is an essential factor for the functioning and economic development of the industrialized world. Energy management has become critical factor for our successive economic prosperity. The energy consumption process frequently needs either DC-AC conversion or AC-DC conversion. The DC-AC conversion finds its major application in uninterrupted power supply (UPS) and renewable energy (RE). In order to supply during power outages, most UPS systems use batteries, usually lead acid, as storage mechanism. The battery is supposed to provide the backup in the absence of the grid supply. However, the voltage provided by the battery alone may not be enough to provide the backup. At first, the battery o/p power which is DC needs to be converted to AC with the help of an inverter. Apparently, the o/p of inverter needs to be step up with the help of step-up transformer to achieve an o/p of 220V, 50Hz [1]. An alternative approach to the same process is by using a power electronic converter called DC-DC boost converter. The boost converters are used in many applications, including photovoltaic systems, UPS, and fuel cell (FC) systems [1]. The standard DC-DC boost converter cannot provide a high gain. As it has been studied in the literature, when the voltage gain is high the efficiency of boost converter reduces. The reason being the losses in the intrinsic resistors of the converter increase when the duty cycle increases, this compromises the performance of the converter [2]-[3]. To overcome this limitation, high gain converter can be used to achieve higher gain [4]-[5]. AC o/p can be achieved with the help of inverter. Also, DC-AC conversion finds its application in RES systems. In such applications like solar photo voltaic (PV) systems, the DC o/p power from PV needs to be converted to AC power [6] &[7].An Inverter circuit is used in cascade with a novel Pulse Width Modulation (PWM) DC-DC hybrid converter [3]&[8]. This cutting-edge PWM DC-DC hybrid converter is primarily utilized to enhance the PV cell voltage profile and reach the necessary i/p voltage level for an Inverter circuit that We have presented single phase 21 and 31-level MLIs In this article, Consider if ‘s‘ number dc i/ps then generalized formula for number of level is 2S+1.The 21-levels of o/p through 10 H-cells this use power for micro grid applications. The schematic block diagram for entire topology is represented in figure 1 and corresponding PV equivalent circuit is mentioned in Figure.2

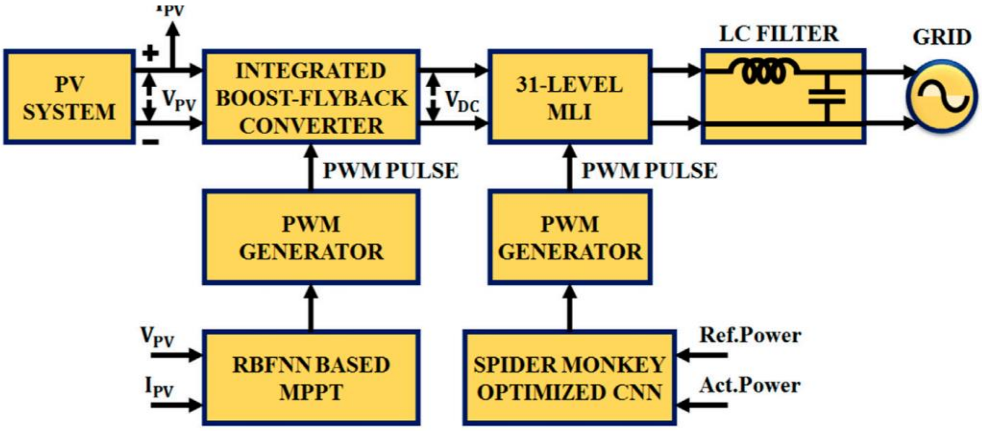

Fig.1: Block diagram for Application of 31 level MLI

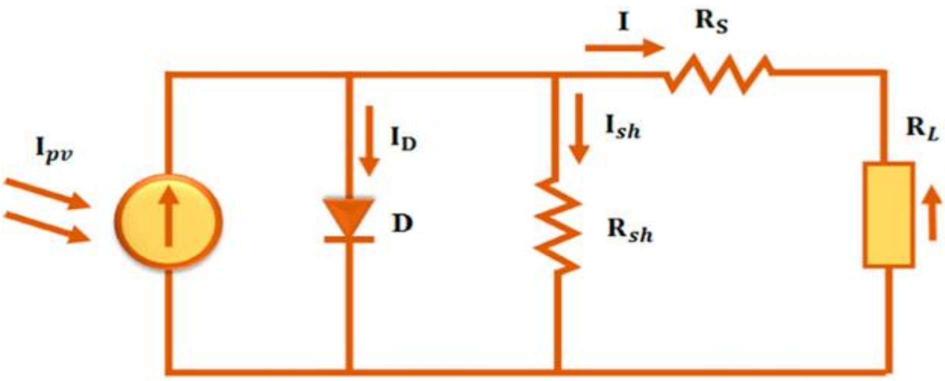

Fig.2: Equivalent circuit of PV array

II. PROPOSED DC-DC IBC:

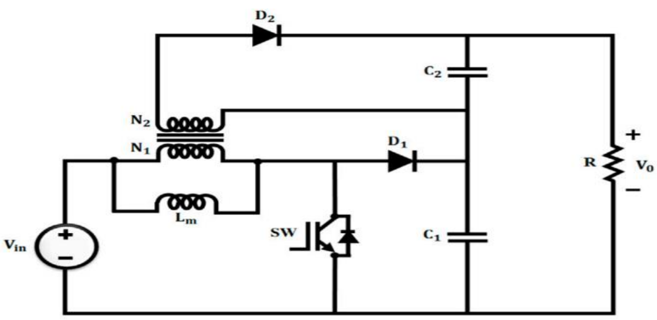

Fig.3: Schematic of IBC

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The above figure 3 represents the schematic of proposed IBC for DC-DC converter.In the mentioned Novel PWM based DC-DC hybrid converter, two inductors L_1 and L_2 are selected with an equal value and is equivalent to L for the equation analysis purpose. The Duty ratio of S_1 was considered as D_1 similarly for S_2 it is D_2.The duty ratio values of both operated switches (S_1 and S_2) were considered as D. The Novel PWM DC-DC hybrid converter can operate in the following modes as mentioned in below figure 4.

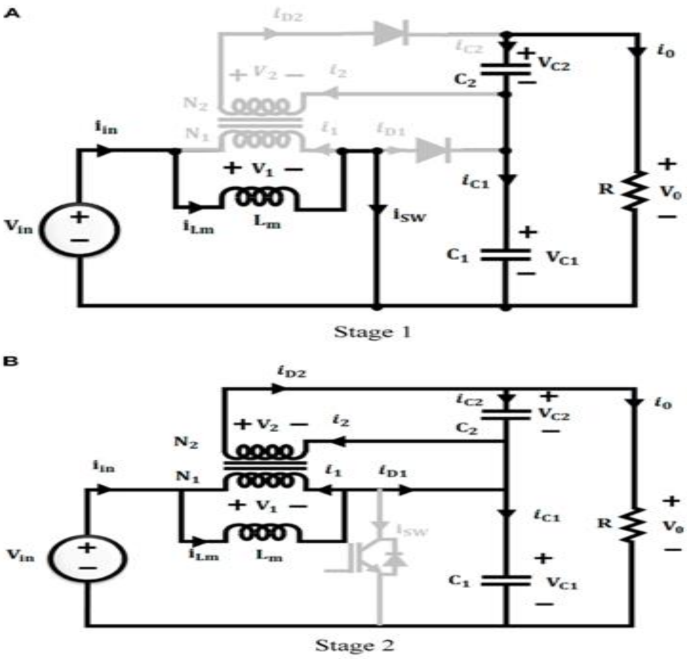

Fig.4: Modes of operation of DC-DC IBC

III.PROPOSEDTOPOLOGYOF31-LEVELINVERTER:

The proposed multilevel inverter uses series connected basic units. The Proposed basic unit for the multilevel inverter is shown in Fig. The basic unit is a combination of two parts which are connected to each other by two switches SP and SN. Each part of the basic unit consists of n/2 dc voltage sources, two unidirectional switches and n/2– 1 bidirectional switches. Such a two-part arrangement for the basic unit allows increasing the number of voltage levels since dc voltage sources with different values can be used in the two parts. It is important to mention that generally in the asymmetric condition the main aim is to maximize the number of voltage levels for a specific number of components. In all of the asymmetric topologies the modularity is lost and the switches do not share the operating voltage in the same manner. In other words, in all of the asymmetric topologies including the proposed topology, switches with different vo1ltage ratings are required. The unidirectional switches consist of an insulated gate bipolar transistor (IGBT) and its anti-parallel diode. The bidirectional switches consist of two IGBTs and their anti- parallel diodes connected in common-emitter form. The bidirectional switches experience bidirectional blocking voltage depending on the different switching combinations. Considering that the basic unit is composed of two parts, it uses n dc voltage sources, n − 2 bidirectional switches and six unidirectional switches. It is notable that the value of the dc

$$V_2 = \frac{n}{2}V_1 + V_1$$

$$V_2 = (\frac{n}{2} + 1)V_1$$

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tage sources in each part of the basic unit are the same but the value of the dc voltage sources of the two parts can be different to generate more output voltage levels. To obtain the maximum number of output voltage levels, V2should be equal to the sum of all of the dc voltage sources with the value of V1 plus the value of one of them. In this way, there would be no redundant switching combination resulting in maximum number of voltage levels.

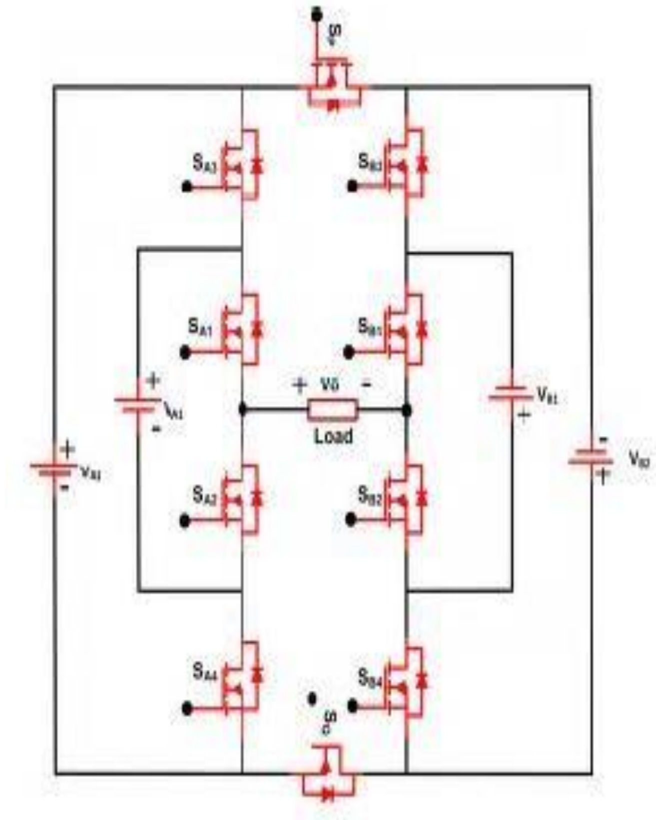

Fig.5: Proposed MLI

It is important to note that in the proposed basic unit, both positive and negative voltage levels can be generated. For the positive voltage levels the switch SP is turned on and for the negative voltage levels the switch SN is turned on. Table.2.1 indicates the switching states of the proposed basic unit. Different output voltage levels can be generated according to this table. Although the proposed basic unit shown in Fig.2.1usesbidirectional switches in addition to unidirectional switches, there are still some unidirectional switches that provide a path for current even if none of the switches are turned on. As the switches S1, S2, Sp and the switches Sn + 1, Sn + 2, Sn are unidirectional, their diodes can conduct the current so that the current path is not disconnected any way. In practice this condition can occur in dead time between the switches. The dead time is time delay between the switching commands of the switches to avoid short circuit. However, in the proposed topology, as there is always a path for current no extra stress is on the switches.

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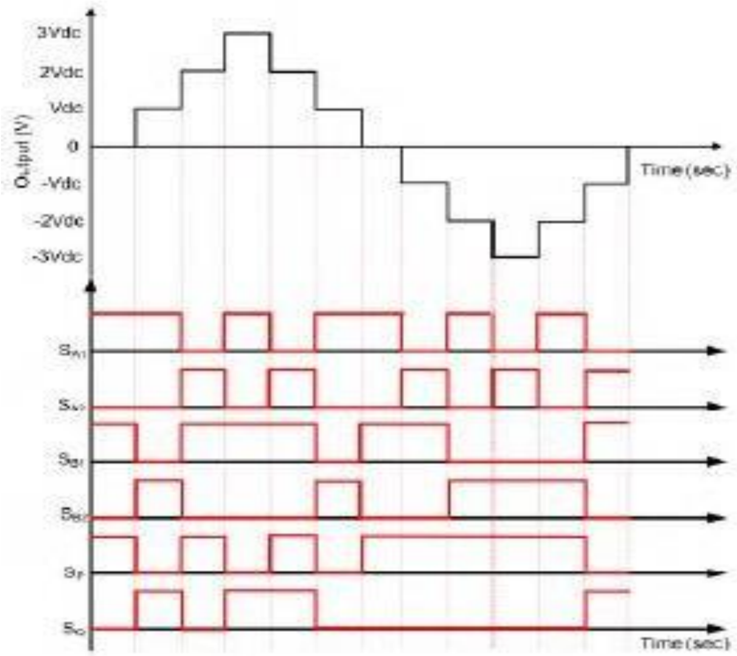

Fig. 6: Typical output and gate pulses of 31-level MLI

Sl.no	Switches On States	Output Voltage
1	$S_{A1}, S_{A3}, S_{B1}, S_{B3}, S_Q$	$V_{A2}+V_{B2}$
2	$S_{A1}, S_{A3}, S_{B2}, S_{B3}, S_Q$	$V_{A2}+V_{B2}-VA1$
3	$S_{A2}, S_{A3}, S_{B1}, S_{B3}, S_Q$	$V_{B2}+V_{A2}-V_{B1}$
4	$S_{A2}, S_{A3}, S_{B2}, S_{B3}, S_Q$	$V_{A2}+V_{B2}-V_{A1}-V_{B1}$
5	$S_{A1}, S_{A3}, S_{B1}, S_{B4}, S_Q$	$V_{A1}+V_{B2}$
6	$S_{A1}, S_{A3}, S_{B2}, S_{B4}, S_Q$	V_{B2}
7	$S_{A2}, S_{A3}, S_{B1}, S_{B4}, S_Q$	$V_{A1}-V_{B1}+V_{B2}$
8	$S_{A2}, S_{A3}, S_{B2}, S_{B4}, S_Q$	$V_{B2}-V_{B1}$
9	$S_{A1}, S_{A4}, S_{B1}, S_{B3}, S_Q$	$V_{A2}+V_{B1}$
10	$S_{A1}, S_{A4}, S_{B2}, S_{B3}, S_Q$	$V_{A2}+V_{B1}-V_{A1}$
11	$S_{A2}, S_{A4}, S_{B1}, S_{B3}, S_Q$	V_{A2}
12	$S_{A2}, S_{A4}, S_{B2}, S_{B3}, S_Q$	$V_{A2}-V_{A1}$
13	$S_{A1}, S_{A4}, S_{B1}, S_{B4}, S_Q$	VA1+VB1
14	$S_{A1}, S_{A4}, S_{B2}, S_{B4}, S_Q$	V_{B1}
15	$S_{A2}, S_{A4}, S_{B1}, S_{B4}, S_Q$	V_{A1}
16	$S_{A1}, S_{A3}, S_{B1}, S_{B3}, S_P$	0
17	$S_{A1}, S_{A3}, S_{B2}, S_{B3}, S_P$	- VA1
18	$S_{A2}, S_{A3}, S_{B1}, S_{B3}, S_P$	$-V_{B1}$
19	$S_{A2}, S_{A3}, S_{B2}, S_{B3}, S_P$	-(VA1+VB1)
20	$S_{A2}, S_{A3}, S_{B1}, S_{B4}, S_P$	$-(V_{A2}-V_{A1})$
21	$S_{A1}, S_{A4}, S_{B1}, S_{B3}, S_P$	$-V_{A2}$
22	$S_{A2}, S_{A4}, S_{B2}, S_{B4}, S_P$	$-(V_{A2}+V_{B1}-V_{A1})$
23	$S_{A2}, S_{A3}, S_{B2}, S_{B4}, S_P$	$-(V_{A2}+V_{B1})$
24	$S_{A1}, S_{A4}, S_{B2}, S_{B3}, S_P$	$-(V_{B2}-V_{B1})$
25	$S_{A1}, S_{A4}, S_{B2}, S_{B3}, S_P$	$-(V_{A1}-V_{B1}+V_{B2})$
26	$S_{A2}, S_{A4}, S_{B1}, S_{B3}, S_P$	$-V_{B2}$
27	$S_{A2}, S_{A4}, S_{B2}, S_{B3}, S_P$	$-(V_{A1}+V_{B2})$
28	$S_{A1}, S_{A4}, S_{B1}, S_{B4}, S_P$	$-(V_{A2}+V_{B2}-V_{A1}-V_{B1})$
29	$S_{A1}, S_{A4}, S_{B2}, S_{B4}, S_P$	$-(V_{B2}+V_{A2}-V_{B1})$
30	$S_{A2}, S_{A4}, S_{B1}, S_{B4}, S_P$	$-(V_{A2}+V_{B2}-V_{A1})$
31	$S_{A2}, S_{A4}, S_B2, S_{B4}, S_P$	$-(V_{A2}+V_{B2})$

Table1. Switching Operation for 31 MLI

IV. INDUCTION MOTOR:

The Induction motor drive is very familiar for agricultural modeling in micro grid application because of its high discharge. A DC motor circuit consists of commutator and brushes so that there is a scope of getting frequent sparks, with this reason the DC motors are normally not preferred in agricultural applications. Because of these reasons generally induction motors are preferred for speed regulated industrial drive applications. Utilizing an induction drive has some technical difficulties as well because it requires two supply conversion steps, AC-DC and DC-AC in V/F control scenarios. Due to its improved electrical properties over other configurations, reversing voltage topology with 31 level converters are typically used an induction motor output in these types of applications.

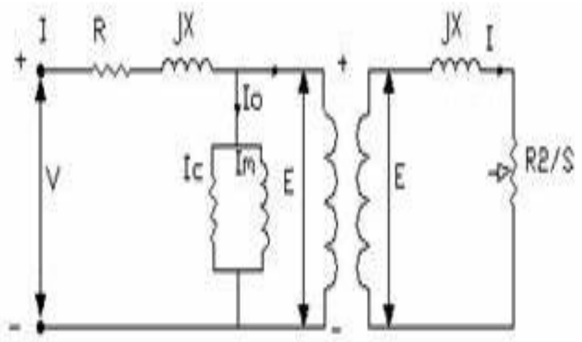

Fig.7: Equivalent circuit of an IM

V. SIMULINK MODEL AND RESULTS:

For verifying the proposed technology, the simulation and experimental results obtained for a31-level inverter based on the proposed topology are presented. The simulation has been carried out for the circuit as shown in figure 4 in MATLAB SIMULINK environment. For experimentation, the gate signals pattern of the switches of the converter is given by repeating sequence stair which provides the switching pulses. The switching pulses are applied to driver circuits that drive the switches. It is important to note that elimination of selected harmonics and total harmonic distortion (THD) minimization are not the aim of this project.

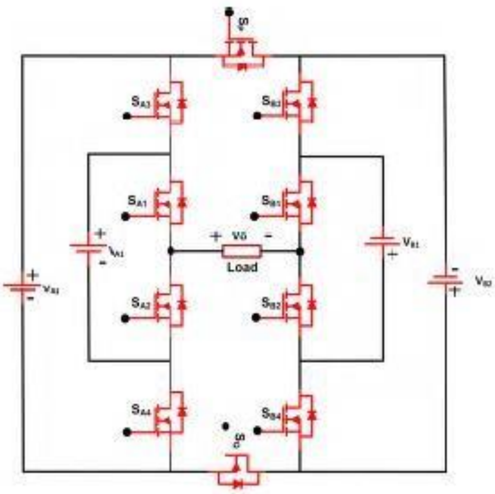

Fig.8:31-level converter based on the proposed topology with two cascaded basic units

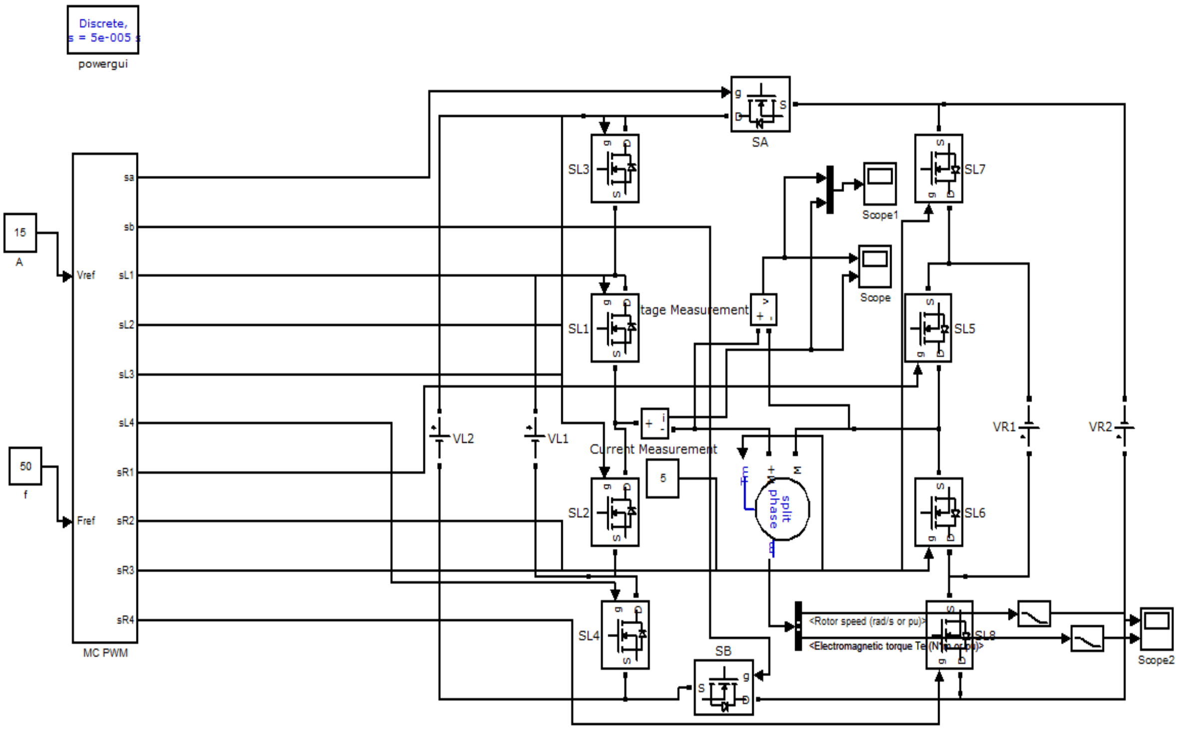

Fig.9: Proposed Simulink topology of 31-level MLI

S.No	Voltage	S1	S2	S3	S4	S5	S6	S7	S8	SA	SB
1	0	1	1	0	0	0	0	1	0	1	1
2	1	0	1	1	0	0	0	1	0	1	1
3	2	0	1	0	0	1	0	1	0	1	1
4	3	1	0	0	1	0	0	1	0	1	1
5	4	0	0	1	1	0	0	1	0	1	1
6	5	0	0	0	1	1	0	1	0	1	1
7	6	1	0	0	0	0	1	1	0	1	1
8	7	0	0	1	0	0	1	1	0	1	1
9	8	0	0	0	0	1	1	1	0	1	1
10	9	1	1	0	0	0	0	0	1	0	1
11	10	0	1	1	0	0	0	0	1	0	1
12	11	0	1	0	0	1	0	0	1	0	1
13	12	1	0	0	1	0	0	0	1	0	1
14	13	0	0	1	1	0	0	0	1	0	1
15	14	0	0	0	1	1	0	0	1	0	1
16	15	1	0	0	0	0	1	0	1	0	1

S.No	Voltage	S1	S2	S3	S4	S5	S6	S7	S8	SA	SB
1	0	0	0	0	0	1	1	0	1	1	1
2	-1	0	0	1	0	0	1	0	1	1	1
3	-2	1	0	0	0	0	1	0	1	1	1
4	-3	0	0	0	1	1	0	0	1	1	1
5	-4	0	0	1	1	0	0	0	1	1	1
6	-5	1	0	0	1	0	0	0	1	1	1
7	-6	0	1	0	0	1	0	0	1	1	1
8	-7	0	1	1	0	0	0	0	1	1	1
9	-8	1	1	0	0	0	0	0	1	1	1
10	-9	0	0	0	0	1	1	1	0	1	0
11	-10	0	0	1	0	0	1	1	0	1	0
12	-11	1	0	0	0	0	1	1	0	1	0
13	-12	0	0	0	1	1	0	1	0	1	0
14	-13	0	0	1	1	0	0	1	0	1	0
15	-14	1	0	0	1	0	0	1	0	1	0

Table-2: Switching operation for Positive and Negative voltages of MLI

The 31-level converter based on the proposed topology uses 10 switches (and 10gate driver circuits), 10 IGBTs and 4 dc voltage sources. The simulation results are shown in Figures.

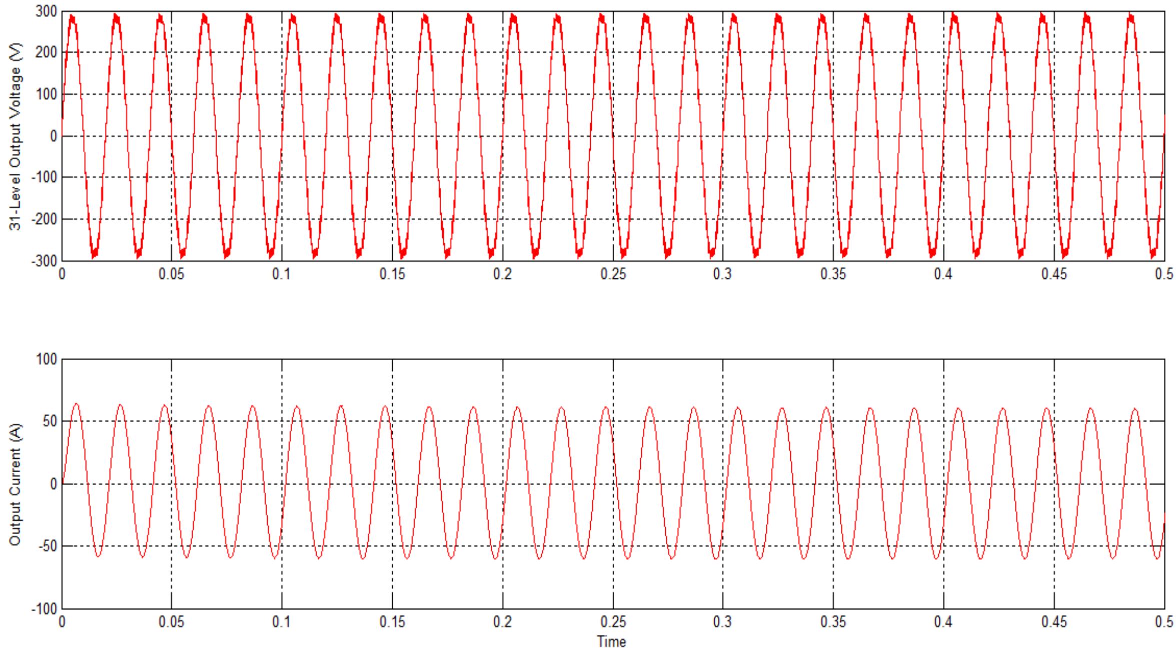

Fig.10: Simulink wave form of Output voltage and Current

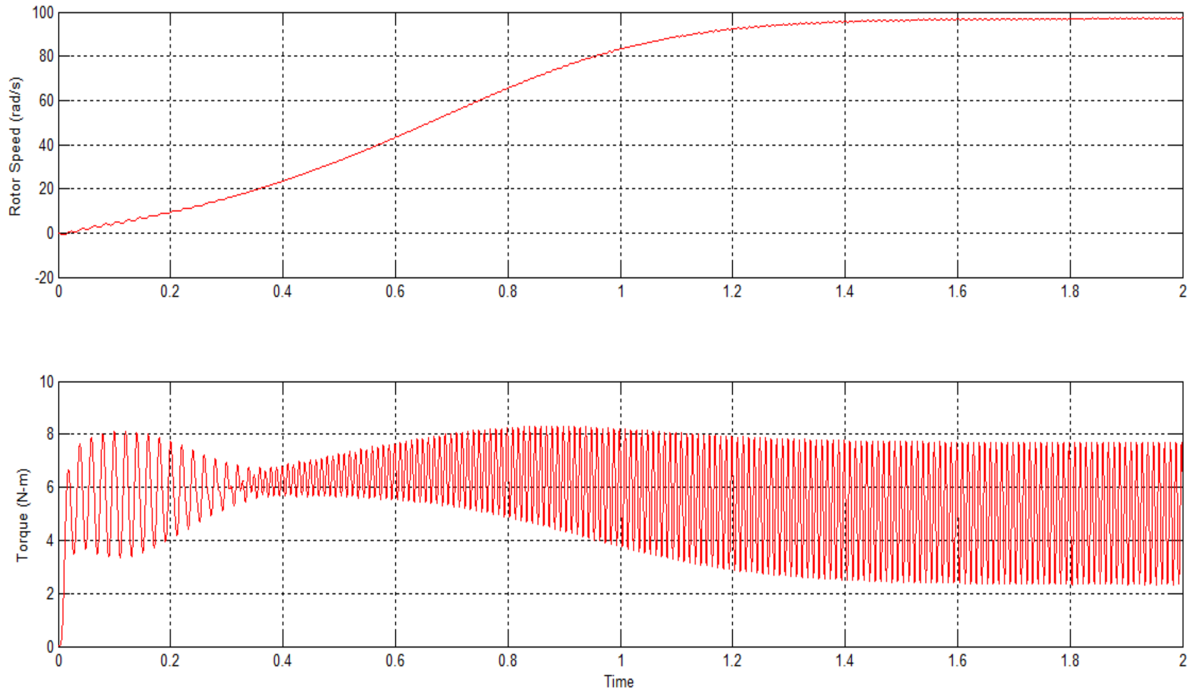

Fig.11: Simulation result of IM Speed and Torque

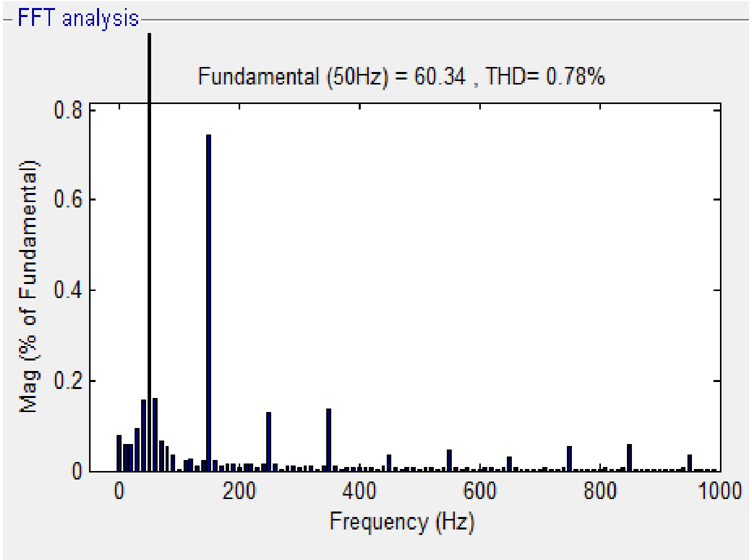

Fig.12: FFT analysis of output voltage

V. CONCLUSION:

From the above presented configurations and their corresponding results it is observed that with an increase in a level of output voltage the respective total harmonic distortion (THD) value reduces. Simultaneously the usage of the requirement of the number switches and their respective driver circuits for designing the topology is also increases. This process makes the circuit design and operation complex. But in this paper the presented novel topology reduces the usage of switches when compared with all the conventional topologies. It also improves the output voltage and efficiency of the circuit. So these type of configurations are highly suitable for micro grid applications because of their added advantages mentioned above.

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