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Designing of Energy Efficient High Speed Opearational Amplifier in CMOS

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Abstract: **-** In this paper we Focuses on the design and simulation of energy-efficient high-speed operational amplifiers using CMOS technology. Our Concept is Design CMC Full Adder with Operational Amplifier. The objective is to achieve high performance with low power consumption by optimizing the design at the transistor level. The IC layout, including several CMOS transistors, capacitors, and resistors arranged to form the operational amplifier circuit. The simulation process includes Layout Versus Schematic (LVS) verification, which ensures that the layout matches the intended schematic design. layout adheres to the manufacturing constraints, indicating a complex circuit designed for high-speed operation Simulations performed on this layout assess key parameters compare power, Delay, Area which are crucial for high-speed Applications. This design's ultimate goal is to provide an operational amplifier with enhanced energy efficiency while maintaining the necessary speed and precision required for advanced CMOS technology applications and We use this in arithmetic log unit after use the Application ALU the power and delay are decreased compared to existing Method.

Keywords*: CMC Full Adder, Operational Amplifier, CMOS, ALU*

1. Introduction

CMC Full adder with Operational Amplifier schematic design focuses on creating a full adder circuit that is based on CMOS technology and integrated with operational amplifiers (OPAMPs) at the output stage to enhance signal, and Power quality. Full adders are fundamental constituents of arithmetic and logic units (ALUs), extensively employed in digital systems for the purpose of binary addition. With the benefits of complementary metal-oxide-semiconductor (CMOS) technology—which has low power dissipation, scalability, and fast switching—this entire adder's schematic has been meticulously constructed.

Three input signals—A, B, and Cin (carry-in)—are used by the circuit to generate two outputs—sum and Cout (carry-out). Combinations of PMOS and NMOS transistors are used the schematic to binary addition Through a sequence of logic operations. This conventional method preserves the essential characteristics of a CMOS full adder while guaranteeing effective charge sharing and signal processing.

Operational amplifiers (OPAMPs) are included at the output stage to enhance the quality of the carry-out and total signals. A crucial buffering mechanism is provided by the OPAMPs, ensuring the signals powering the circuit's subsequent stages have little noise distortion and a short propagation delay. Additionally, the OPAMPs enhance the circuit's driving Capacity, which is critical in high-speed applications with significant capacitive loads.

In order to balance power and performance, the design makes use of transistor-level optimization, carefully choosing the widths and lengths of the PMOS and NMOS transistors. The circuit is designed to meet low power consumption needs without sacrificing speed thanks to a schematic that minimizes the power-delay product (PDP).

In order to provide exact amplification and little offset in the output signals, appropriate biasing and matching in the OPAMPs are also critical design factors. Transistors are arranged logically and systematically in both the OPAMP and full adder stages to provide shorter signal lines and less parasitic capacitance for better performance.

CMC Full adder schematic's operational functionality is intended to function at nanoscale technology nodes,

which are becoming more and more common in integrated circuits of the contemporary. Scalability is made possible by the technology selection, which qualifies this design for a variety of uses, including DSP microprocessors, and low-power portable devices.

For simulation we use Cadence Virtuoso tool comparable platform to confirm that the entire adder circuit functions. Propagation delay, power consumption, and output voltage levels are the main topics of the simulation. The time response of the circuit at high frequencies and the enhanced signal quality resulting from the use of operational amplifiers at the output stage are both demonstrated by the simulation results.

Following the schematic, the CMOS full adder layout is designed to minimize parasitic effects and optimize area. Cadence Layout Editor is used for precise transistor placement, routing, and power rail design. Particular attention is paid to matching device geometries, especially in the OPAMP's differential pairs, ensuring balanced and precise sum and carry-out outputs.

The physical layout accurately reflects the schematic, Layout vs. Schematic (LVS) verification is conducted. LVS checks confirm electrical connectivity, device sizes, and network equivalence between the schematic and layout, ensuring the fabricated circuit functions as Calculated and meets performance and reliability standard.

We Use an Application for This Arithmetic and logic Unit. We Design Our Existing Method Conventional Mirror Full adder and Proposed Method Conventional Mirror Full Adder with Operational Amplifier in Between the Designing a ALU We Use Different kinds of Logic Gates Like AND, OR, XOR, 4*1MULTIPLIER.After Design All the Gates We Add Our Conventional Mirror Full Adeer and combined all the Gates. We Generate a Schematic and also design Replace Above Full Adder with Conventional Mirror Full Adder with OP AMP to Generate a Schematics and Simulation. This is We Design in Cadence Virtuoso 28nm Technology.

2. Objectives

some potential objectives for our designing energy-efficient, high-speed operational amplifiers in CMOS, integrating the use of CMOS-based full adder circuits for ALU design:

1. Design and Develop Energy-Efficient Op- Amps: To design operational amplifiers that operate efficiently at low power while achieving high-speed performance, particularly in nanometer-scale CMOS technology.
2. Enhance ALU Performance Using CMOS Full Adder Circuits: To improve arithmetic unit performance by integrating CMOS-based full adder circuits, focusing on minimal power consumption and high-speed data processing.
3. Optimize for High-Speed Applications: To ensure that the operational amplifier design supports high-frequency applications, targeting reduced delay and faster signal processing suitable for modern computing demands.
4. Integrate Image Processing Applications: To explore the application of CMOS full adders in image processing tasks, potentially optimizing tasks related to image data processing, enhancing throughput, and reducing latency.
5. Validate with Simulation and Measurement**: To perform simulations and measurements that validate the effectiveness, speed, and energy efficiency of the proposed amplifier and full adder designs, with a focus on ALU integration for practical applications.
6. Contribute to Scalable and Compact CMOS Design**: To propose a design methodology that aligns with the requirements for miniaturization and integration in advanced nanometer CMOS technology nodes, enabling scalable and compact layouts.

3. Methods

A.CMC Full adder

Conventional mirror full adder is a fundamental component in digital electronics, essential for binary addition in arithmetic circuits. A full adder takes three binary inputs: two significant bits (A and B) and a carry-in bit (Cin). It produces two outputs: the sum (S) and the carry-out (Cout).

In the terms of implementation, the mirror full adder utilizes basic logic gates, including XOR, AND, and OR gates. The first XOR gate combines inputs A and B to generate an intermediate signal. This signal is then fed into a second XOR gate along with Cin to produce the final sum. Simultaneously, two AND gates generate the partial carry values: one from inputs A and B, and the other from the intermediate output and Cin. These partial carries are then combined using an OR gate to yield the final carry-out.

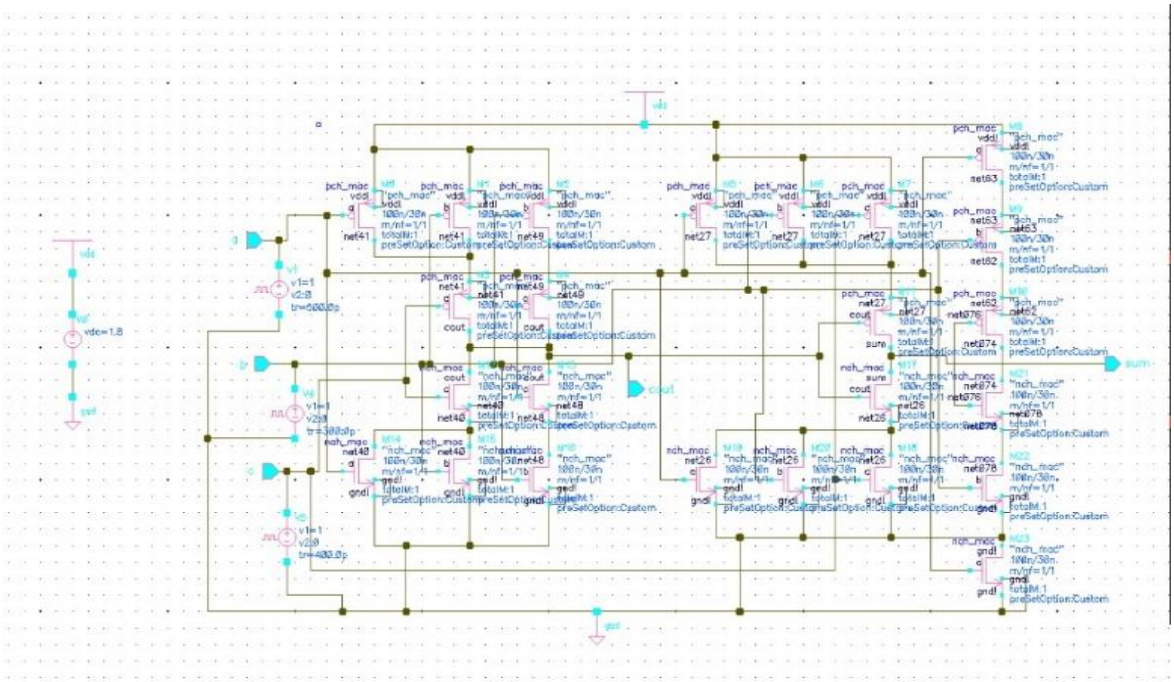


Fig1a. CMC Full Adder

The design of the conventional mirror full adder can be summarized through its truth table, which outlines the outputs for all possible input combinations. This table demonstrates the adder's ability to produce correct results across various binary inputs, establishing its reliability and efficiency in digital systems. Further more understanding the mirror full adder serves as a foundational step toward designing more complex arithmetic circuits.

The conventional mirror full adder remains the Crucial element in digital circuit design, illustrating the principles of binary addition through straightforward logic operations. Its efficient design makes it indispensable for applications ranging from simple calculators to advanced computing systems, where arithmetic operations play a vital role. Continued exploration of such fundamental circuits is essential for advancing digital technology.

B.CMC Full adder With Operational Amplifier

An operational amplifier is used to Improve the performance of the full adder Through improving signal strength, providing better voltage swings, and increase the gain of the circuit. OPAMPs are particularly useful in high-speed and low-power applications as they offer excellent Noise reduction.

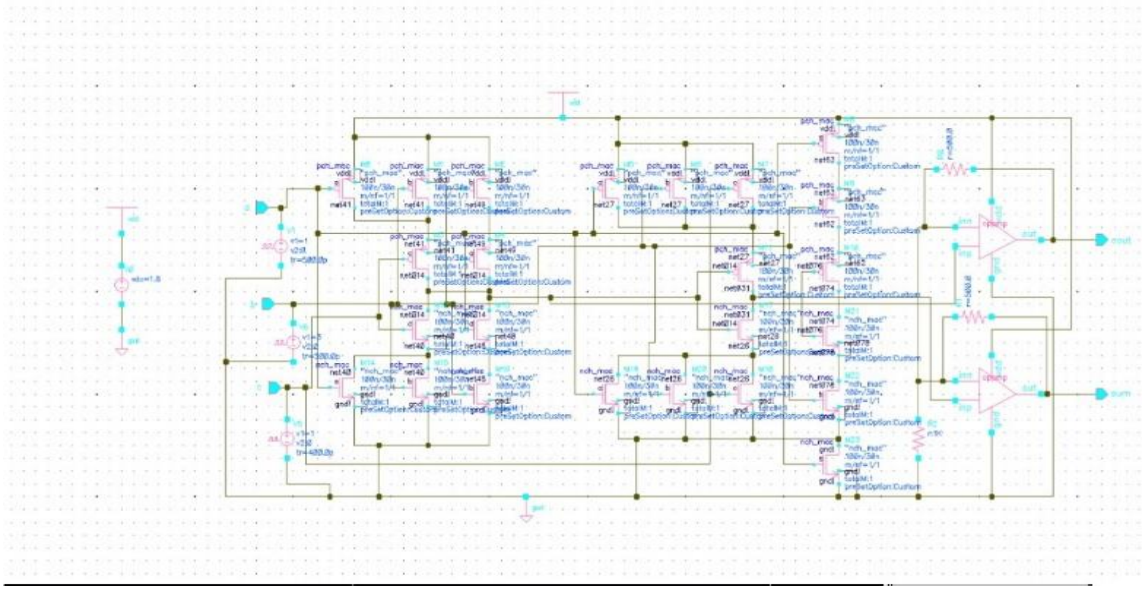


Fig1b. CMC Full Adder with Operational Amplifier

In the CMOS full adder with OPAMP, the sum and carry signals can be fed into the OPAMP for amplification before driving subsequent stages in the circuit. The improvement of Overall Circuit by Reducing Propagation Delay for Reducing the Delay by Signal Propagation across Increase Signal Integrity. In this Technology Voltage Levels are Degrade Due to Noise. The OP AMP ensures the Output Signals Strong and Proper Voltage Levels Improving Overall System Reliability. OPAMPs, when designed appropriately, can significantly reduce the dynamic power consumption of the full adder, as they reduce the need for repeated charging and discharging of capacitive loads in subsequent stages.

C. Designing of ALU Using CMC Full Adder

We are Designing an ALU for the CMC Full Adder for where We use ALU enables complex computations, including binary arithmetic, error correction, signal processing Design of a CMC Full Adder Multiple Logic Gates Like AND, OR, XOR.

The instances AND, OR, XOR, MUX are Connected to implement Boolean Functions. The inputs are a, b and c are Through these Gates and Generate the Sum and Carry Outputs.

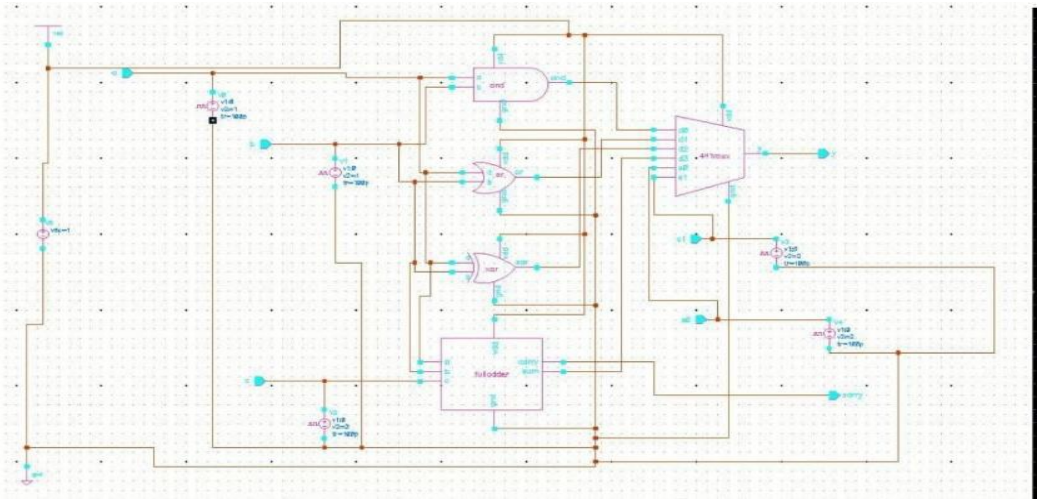


Fig1c. Designing of ALU using CMC Full Adder

Full Adder is Arithmetic Operation in this Circuit inputs are connected for Full Adder is a, b, c and Outputs are Sum, Carry. The two Outputs of Full Adder is Connected to the input of Multiplexer it Generates Output of ALU. This Design we take from Reference (11) for Implementing ALU Design.

Multiplexer is a Main Role in this Design it is used to All Gates are Connected with Multiplexer to Generate output the inputs are for MUX is d0, d1, d2, d3, s0, s1 these inputs to generate output Carry, y.

D. Designing of ALU Using CMC Full Adder with Operational Amplifier

We are Designing an ALU for the CMC Full Adder with Operational Amplifier inputs are for Full Adder with Operational Amplifier a, b, c and Basic Logic Gates for the Designing Alu for Full Adder with Operational Amplifier OR, AND, XOR Gates.

Op-Amp is used to amplify the sum and carry signals, enhancing the performance by improving speed and reducing noise in the circuit. This is particularly useful in high-speed applications and provides improved signal integrity CMOS technologies.

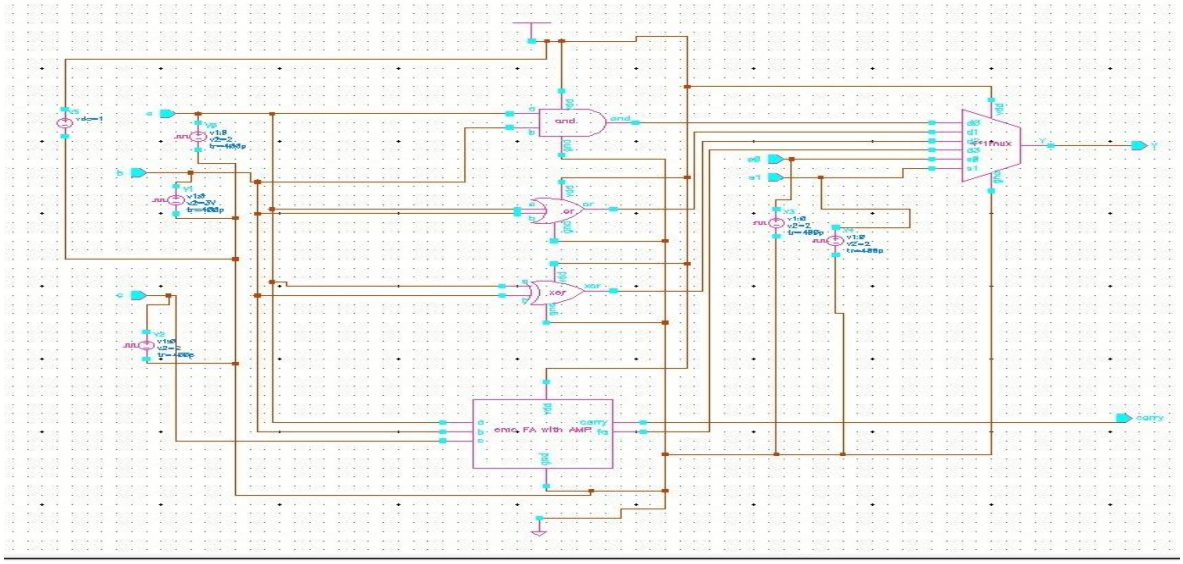


Fig1d. Designing of ALU Using CMC Full Adder with Operational Amplifier

The Multiplexer are Take four Inputs and two Selection lines that are d0, d1, d2, d3 and s0, s1 these inputs to pass the output. s0, s1 are the Control Signals for the MUX These are allow for Dynamic Selection of Data Paths.

Uses of this CMOS full adder with an operational amplifier to enhance the accuracy and speed of the signal Outputs. We could use this circuit in digital arithmetic units and fast addition is required, possibly in processors or DSP systems.

3. Results

A. Simulation for CMC Full Adder

simulation results illustrate the transient response of a CMOS-based full adder Circuit, the relationship between the input signals (`a`, `b`, and `c`) and the corresponding outputs, `sum` and `carry-out` (Cout). The X-axis represents time in nanoseconds, while the Y-axis displays the voltage levels that indicate binary logic states, with high voltage (approximately 1.8V) representing logic high, and low voltage (1 to 0v) representing logic low. simulation traces for the inputs `a`, `b`, and `c` demonstrate binary transitions that feed into the full adder logic. These inputs switch at specific intervals, and the resulting output waveforms for `sum` (in blue) and `carry-out` (in magenta) correspond to the logical operations of the full adder. The `sum` output is

computed as the XOR (⊕) of the three inputs, following the equation: `sum = a ⊕ b ⊕ c`. Similarly, the carry-out is determined by the majority logic of the inputs.

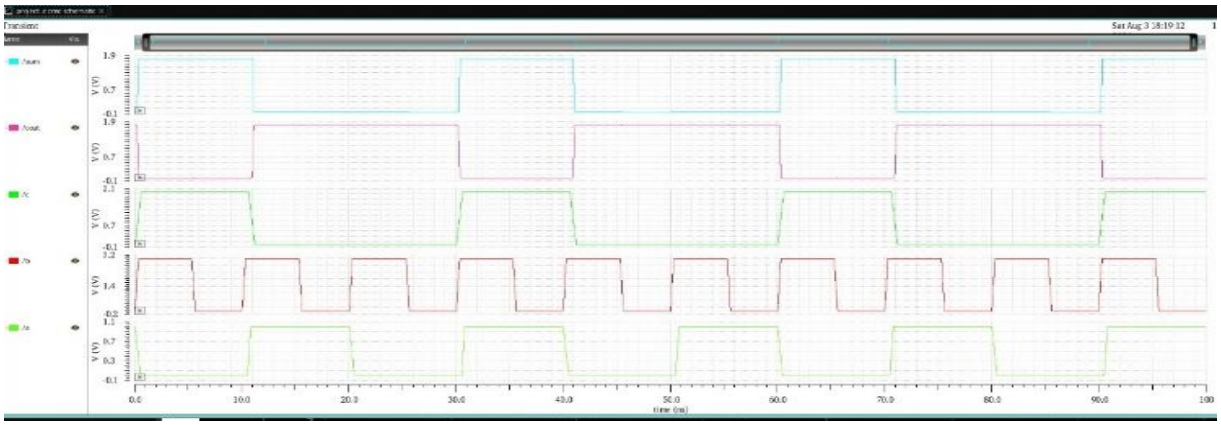


Fig2a. Simulation Result for CMC Full Adder

simulation results verify that the outputs `sum` and `cout` correctly follow the expected logic over the given time intervals, confirming that the CMOS full adder performs reliably in high-speed applications. This validation is for designing energy-efficient circuits, particularly in modern CMOS technologies where power efficiency and performance are critical factors for digital systems. circuit's behavior under various input combinations demonstrates its integration into larger digital processing systems.

Analysis is highlighting the effective design of the CMOS full adder, emphasizing its potential for high-speed, low-power digital applications.

B. Simulation for CMC Full Adder with Operational Amplifer

In Cadence Virtuoso 28nm, the CMOS full adder circuit integrated with operational amplifiers (OPAMPs) was simulated. transient analysis was used to see how the sum and carry-out (c out) signals behaved dynamically. Following the application of input Signals A, B, and C, performance metrics such as rise/fall times, power consumption, and propagation delay were extracted. Through the reduction of noise and amplification of weak outputs, the OPAMP greatly enhanced signal integrity.

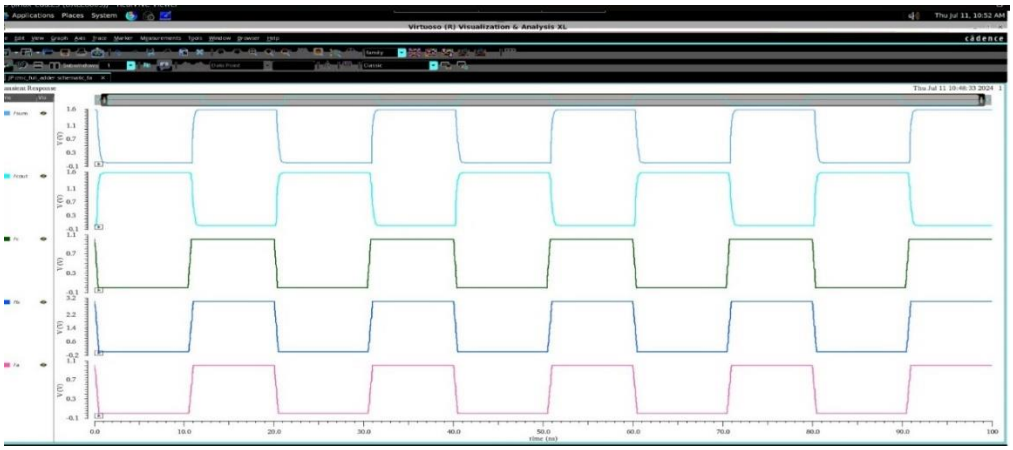


Fig2b. Simulation for CMC Full Adder with Operational Amplifier

The waveform results validated the design for high-speed, low-power applications by confirming clean and reliable sum and Cout signals. The efficiency and resilience of the circuit were validated by the simulation results, which closely matched theoretical prediction.

C. Simulation for ALU Application for CMC Full Adder

The Simulation Focuses on timing and performance of ALU.

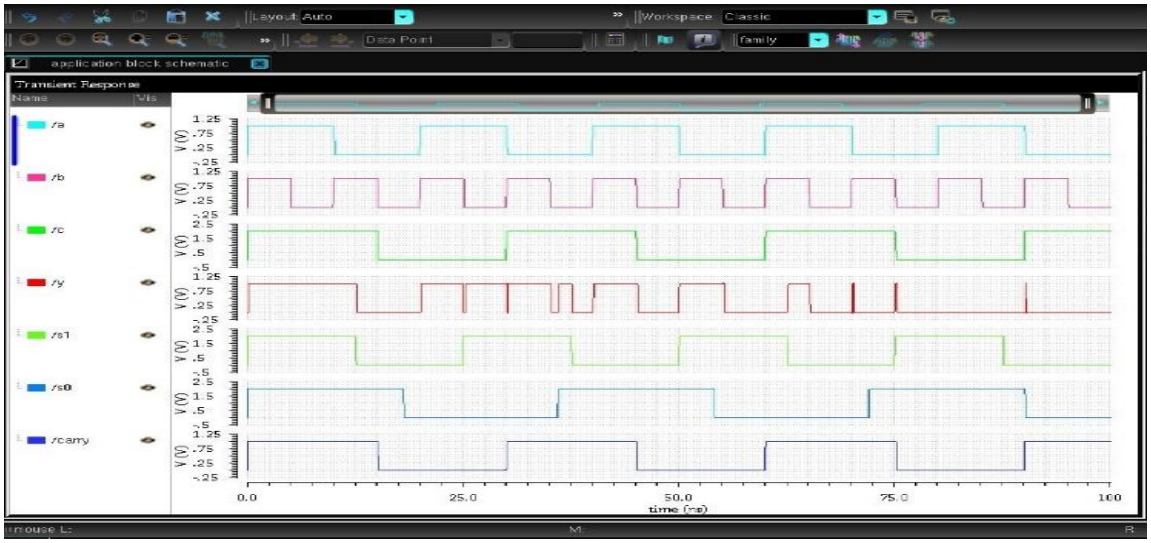


Fig2c.Simulation for Application ALU Using CMC Full Adder

The timing behavior is analyzed to determine the total computation time for multi-bit addition. Power consumption is another important factor, and the simulation tracks the power usage of the ALU during different operations

D. Simulation for ALU Application for CMC Full Adder with Operational Amplifier

This simulation focuses on the timing and power consumption of the ALU, especially with the full adder with Op-Amp. The timing analysis evaluates how quickly the carry propagates through the full adder and how the operational amplifier impacts the overall delay of the circuit. Delay introduced by the Op-Amp is measured and power consumption of the ALU is tracked during different operations.

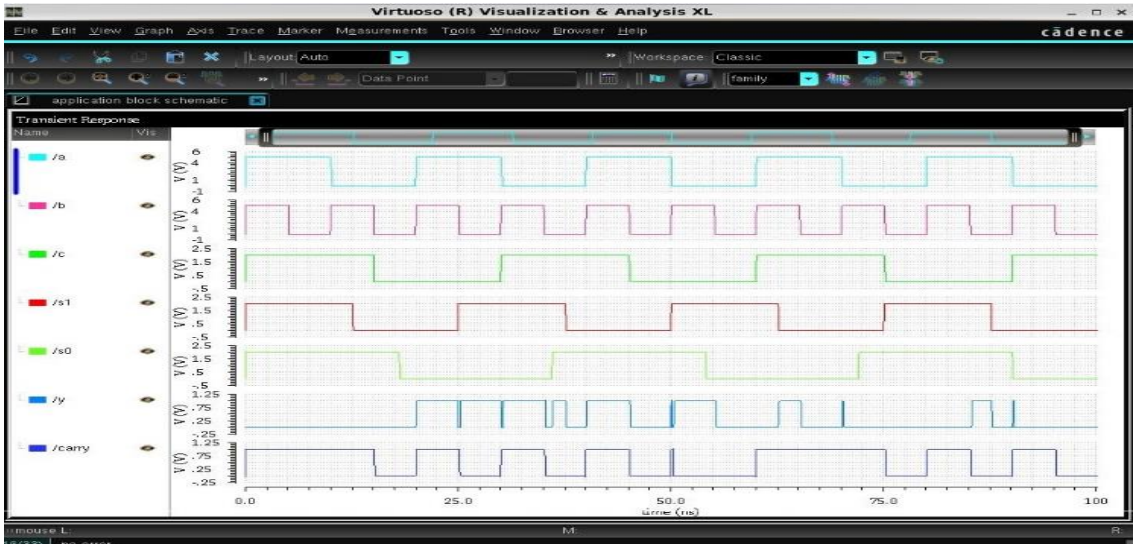


Fig2d. Simulation for Application ALU Using CMC Full Adder with Operational Amplifier

The Op-Amp, being an Analog component, consumes additional power compared to purely digital Components. The simulation ensures that the power overhead introduced by the Op-Amp that the ALU operates within power limits for energy-efficient designs.

E. Layout

CMOS complete adder circuit combined with operational amplifiers (OPAMPs) is depicted in the layout. Standard CMOS layout techniques are used in the design, with discrete zones for PMOS and NMOS transistors coupled in a complementary way to carry out the logic. With its connections for inputs (A, B, and Cin) and matching logic gates, the left portion of the arrangement seems to be the

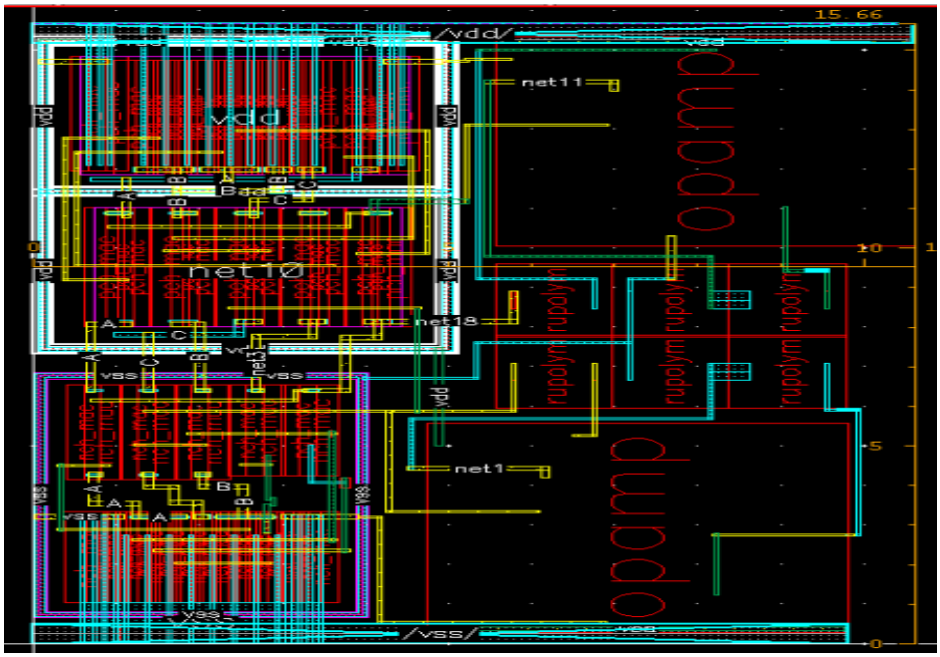


Fig3: Layout for CMC Full Adder with Operational Amplifier

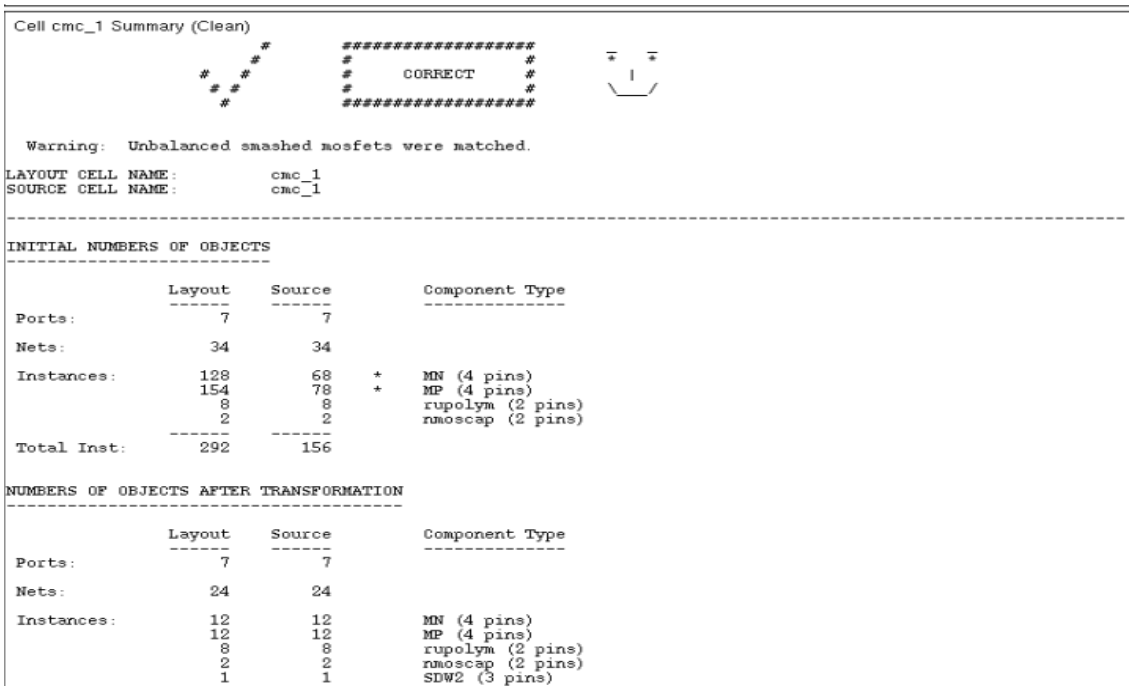
central component of the entire adder. The circuit is powered via the VDD (power supply) and VSS (ground) wires, which are located at the top and bottom. To improve signal strength and stability, the OPAMPs are positioned on the right and coupled to the sum and carry-out outputs. Transistors and other components are connected by metal layers, which are shown as coloured lines.

F. LVS Report for CMC Full Adder with Operational Amplifier

An essential step in confirming that integrated circuits match the original schematic design is the LVS (Layout Versus Schematic) Check. By identifying differences between the schematic and the sketched layout, the LVS process verifies the integrity of the design prior to manufacture. The layout and source netlists are consistent with the total number of items that are correctly matched, as confirmed by the LVS summary for the cell cmc_1 in this report. The alert "Unbalanced smashed Mosfets were matched" indicates that although the tool was able to align the MOSFET structures, there may have been adjustments or less-than-ideal During the Matching Process.

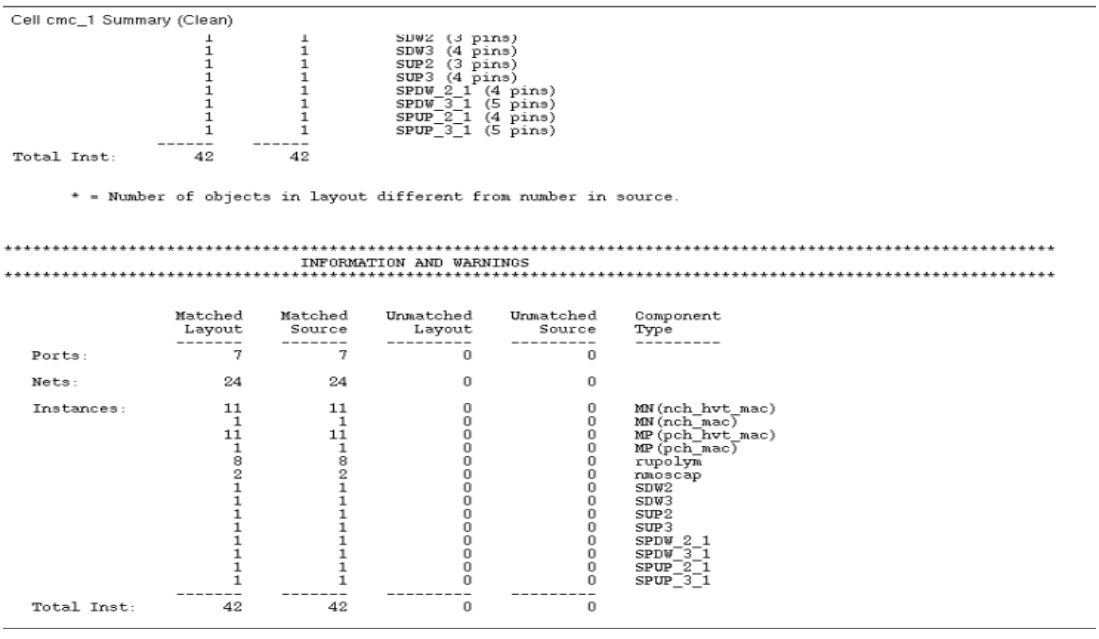
Seven ports, thirty-four nets, and two hundred and ninety-two instances of various components—including four-pin NMOS (MN) and PMOS (MP) transistors and capacitors such are included in the first object count. These figures show us many devices are integrated and how complex the design is overall. The total number of instances was lowered to 156 following transformation (optimizations and modifications made by the LVS tool), with matched nets and ports displaying consistency in both the layout and source. Reducing redundant or mismatched components, the instance counts for NMOS and PMOS transistors were aligned (12NMOS,12PMOS).

Confirming the circuit's dependability and preparation for manufacture requires a proper match between the layout and schematic following transformation.



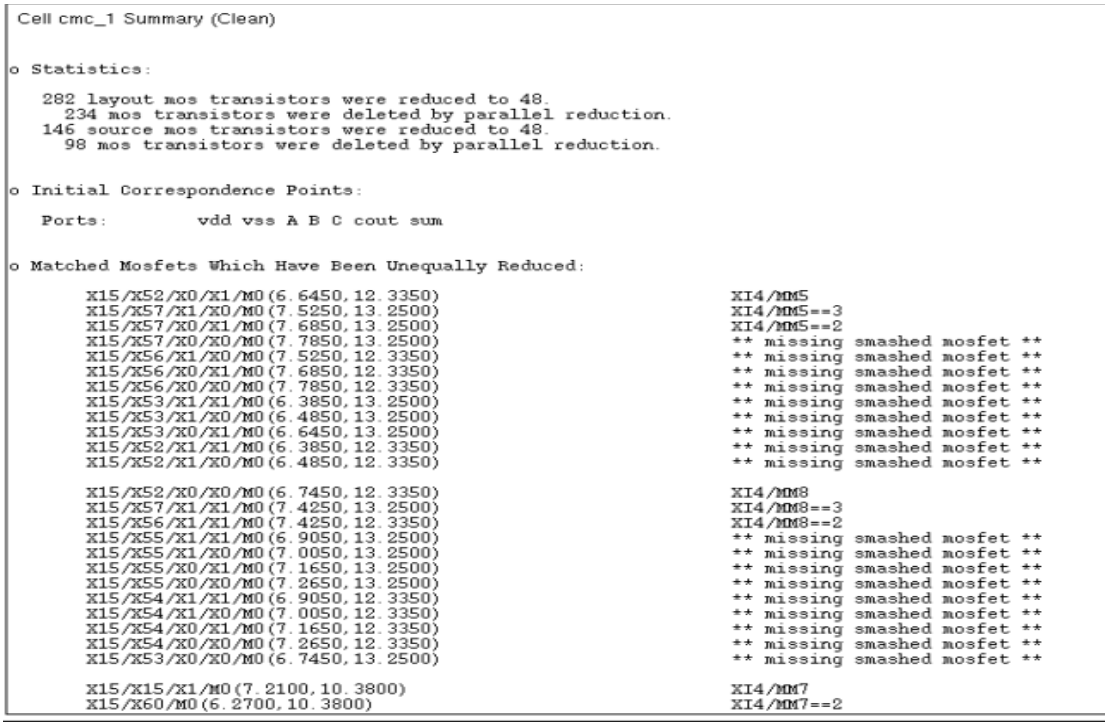
```
Cell cmc_1 Summary (Clean)
                    #       ###################
                  #         #                 #
                #   #       #     CORRECT     #
                  # #       #                 #
                    #       ###################

  Warning:  Unbalanced smashed mosfets were matched.

LAYOUT CELL NAME:          cmc_1
SOURCE CELL NAME:          cmc_1
------------------------------------------------------------------------------------------------------------------------

INITIAL NUMBERS OF OBJECTS
--------------------------

                Layout    Source          Component Type
                ------    ------          --------------
 Ports:              7         7

 Nets:              34        34

 Instances:        128        68    *     MN (4 pins)
                   154        78    *     MP (4 pins)
                     8         8          rupolym (2 pins)
                     2         2          nmoscap (2 pins)
                ------    ------
 Total Inst:       292       156

NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------

                Layout    Source          Component Type
                ------    ------          --------------
 Ports:              7         7

 Nets:              24        24

 Instances:         12        12          MN (4 pins)
                    12        12          MP (4 pins)
                     8         8          rupolym (2 pins)
                     2         2          nmoscap (2 pins)
                     1         1          SDW2 (3 pins)
```

Fig4a: LVS Report



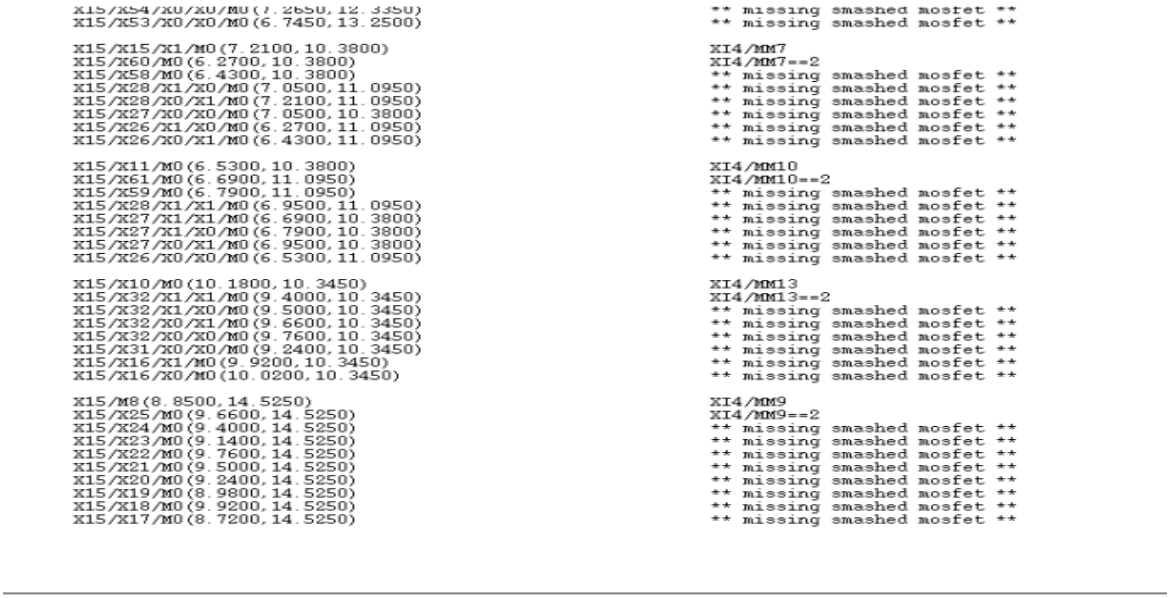
```
Cell cmc_1 Summary (Clean)
                     1         1          SDW2 (3 pins)
                     1         1          SDW3 (4 pins)
                     1         1          SUP2 (3 pins)
                     1         1          SUP3 (4 pins)
                     1         1          SPDW_2_1 (4 pins)
                     1         1          SPDW_3_1 (5 pins)
                     1         1          SPUP_2_1 (4 pins)
                     1         1          SPUP_3_1 (5 pins)
                ------    ------
 Total Inst:        42        42

       * = Number of objects in layout different from number in source.

**********************************************************************************************************************
                                        INFORMATION AND WARNINGS
**********************************************************************************************************************

                Matched   Matched   Unmatched   Unmatched   Component
                 Layout    Source     Layout      Source     Type
                -------   -------   ---------   ---------   ---------
   Ports:             7         7           0           0
   Nets:             24        24           0           0
   Instances:        11        11           0           0   MN(nch_hvt_mac)
                      1         1           0           0   MN(nch_mac)
                     11        11           0           0   MP(pch_hvt_mac)
                      1         1           0           0   MP(pch_mac)
                      8         8           0           0   rupolym
                      2         2           0           0   nmoscap
                      1         1           0           0   SDW2
                      1         1           0           0   SDW3
                      1         1           0           0   SUP2
                      1         1           0           0   SUP3
                      1         1           0           0   SPDW_2_1
                      1         1           0           0   SPDW_3_1
                      1         1           0           0   SPUP_2_1
                      1         1           0           0   SPUP_3_1
                -------   -------   ---------   ---------
   Total Inst:       42        42           0           0
```

Fig4b: LVS Report



```
Cell cmc_1 Summary (Clean)


o Statistics:

   282 layout mos transistors were reduced to 48.
     234 mos transistors were deleted by parallel reduction.
   146 source mos transistors were reduced to 48.
     98 mos transistors were deleted by parallel reduction.


o Initial Correspondence Points:

   Ports:          vdd vss A B C cout sum


o Matched Mosfets Which Have Been Unequally Reduced:

       X15/X52/X0/X1/M0(6.6450,12.3350)                    XI4/MM5
       X15/X57/X1/X0/M0(7.5250,13.2500)                    XI4/MM5==3
       X15/X57/X0/X1/M0(7.6850,13.2500)                    XI4/MM5==2
       X15/X57/X0/X0/M0(7.7850,13.2500)                    ** missing smashed mosfet **
       X15/X56/X1/X0/M0(7.5250,12.3350)                    ** missing smashed mosfet **
       X15/X56/X0/X1/M0(7.6850,12.3350)                    ** missing smashed mosfet **
       X15/X56/X0/X0/M0(7.7850,12.3350)                    ** missing smashed mosfet **
       X15/X53/X1/X1/M0(6.3850,13.2500)                    ** missing smashed mosfet **
       X15/X53/X1/X0/M0(6.4850,13.2500)                    ** missing smashed mosfet **
       X15/X53/X0/X1/M0(6.6450,13.2500)                    ** missing smashed mosfet **
       X15/X52/X1/X1/M0(6.3850,12.3350)                    ** missing smashed mosfet **
       X15/X52/X1/X0/M0(6.4850,12.3350)                    ** missing smashed mosfet **

       X15/X52/X0/X0/M0(6.7450,12.3350)                    XI4/MM8
       X15/X57/X1/X1/M0(7.4250,13.2500)                    XI4/MM8==3
       X15/X56/X1/X1/M0(7.4250,12.3350)                    XI4/MM8==2
       X15/X55/X1/X1/M0(6.9050,13.2500)                    ** missing smashed mosfet **
       X15/X55/X1/X0/M0(7.0050,13.2500)                    ** missing smashed mosfet **
       X15/X55/X0/X1/M0(7.1650,13.2500)                    ** missing smashed mosfet **
       X15/X55/X0/X0/M0(7.2650,13.2500)                    ** missing smashed mosfet **
       X15/X54/X1/X1/M0(6.9050,12.3350)                    ** missing smashed mosfet **
       X15/X54/X1/X0/M0(7.0050,12.3350)                    ** missing smashed mosfet **
       X15/X54/X0/X1/M0(7.1650,12.3350)                    ** missing smashed mosfet **
       X15/X54/X0/X0/M0(7.2650,12.3350)                    ** missing smashed mosfet **
       X15/X53/X0/X0/M0(6.7450,13.2500)                    ** missing smashed mosfet **

       X15/X15/X1/M0(7.2100,10.3800)                       XI4/MM7
       X15/X60/M0(6.2700,10.3800)                          XI4/MM7==2
```

Fig4c: LVS Report



```
Cell cmc_1 Summary (Clean)
       X15/X54/X0/X0/M0(7.2650,12.3350)                    ** missing smashed mosfet **
       X15/X53/X0/X0/M0(6.7450,13.2500)                    ** missing smashed mosfet **

       X15/X15/X1/M0(7.2100,10.3800)                       XI4/MM7
       X15/X60/M0(6.2700,10.3800)                          XI4/MM7==2
       X15/X58/M0(6.4300,10.3800)                          ** missing smashed mosfet **
       X15/X28/X1/X0/M0(7.0500,11.0950)                    ** missing smashed mosfet **
       X15/X28/X0/X1/M0(7.2100,11.0950)                    ** missing smashed mosfet **
       X15/X27/X0/X0/M0(7.0500,10.3800)                    ** missing smashed mosfet **
       X15/X26/X1/X0/M0(6.2700,11.0950)                    ** missing smashed mosfet **
       X15/X26/X0/X1/M0(6.4300,11.0950)                    ** missing smashed mosfet **

       X15/X11/M0(6.5300,10.3800)                          XI4/MM10
       X15/X61/M0(6.6900,11.0950)                          XI4/MM10==2
       X15/X59/M0(6.7900,11.0950)                          ** missing smashed mosfet **
       X15/X28/X1/X1/M0(6.9500,11.0950)                    ** missing smashed mosfet **
       X15/X27/X1/X1/M0(6.6900,10.3800)                    ** missing smashed mosfet **
       X15/X27/X1/X0/M0(6.7900,10.3800)                    ** missing smashed mosfet **
       X15/X27/X0/X1/M0(6.9500,10.3800)                    ** missing smashed mosfet **
       X15/X26/X0/X0/M0(6.5300,11.0950)                    ** missing smashed mosfet **

       X15/X10/M0(10.1800,10.3450)                         XI4/MM13
       X15/X32/X1/X1/M0(9.4000,10.3450)                    XI4/MM13==2
       X15/X32/X1/X0/M0(9.5000,10.3450)                    ** missing smashed mosfet **
       X15/X32/X0/X1/M0(9.6600,10.3450)                    ** missing smashed mosfet **
       X15/X32/X0/X0/M0(9.7600,10.3450)                    ** missing smashed mosfet **
       X15/X31/X0/X0/M0(9.2400,10.3450)                    ** missing smashed mosfet **
       X15/X16/X1/M0(9.9200,10.3450)                       ** missing smashed mosfet **
       X15/X16/X0/M0(10.0200,10.3450)                      ** missing smashed mosfet **

       X15/M8(8.8500,14.5250)                              XI4/MM9
       X15/X25/M0(9.6600,14.5250)                          XI4/MM9==2
       X15/X24/M0(9.4000,14.5250)                          ** missing smashed mosfet **
       X15/X23/M0(9.1400,14.5250)                          ** missing smashed mosfet **
       X15/X22/M0(9.7600,14.5250)                          ** missing smashed mosfet **
       X15/X21/M0(9.5000,14.5250)                          ** missing smashed mosfet **
       X15/X20/M0(9.2400,14.5250)                          ** missing smashed mosfet **
       X15/X19/M0(8.9800,14.5250)                          ** missing smashed mosfet **
       X15/X18/M0(9.9200,14.5250)                          ** missing smashed mosfet **
       X15/X17/M0(8.7200,14.5250)                          ** missing smashed mosfet **
```

Fig4d: LVS Report

Seven ports, thirty-four nets, and two hundred and ninety-two instances of various components—including four-pin NMOS (MN) and PMOS (MP) transistors and capacitors such are included in the first object count. These figures show us many devices are integrated and how complex the design is overall.

The total number of instances was lowered to 156 following transformation (optimizations and modifications made by the LVS tool), with matched nets and ports displaying consistency in both the layout and source. Reducing redundant or mismatched components, the instance counts for NMOS and PMOS transistors were

aligned (12 NMOS, 12 PMOS).

The circuit's dependability Is Correctly and preparation for manufacture requires a proper match between the layout and schematic following transformation.

4. Discussion

A.Power Consumption

Compared to the conventional Mirror Full Adder the Conventional Mirror Full Adder with Operational Amplifier the power consumption is Reduced to 50% the power is 1.37 Wm. Designing of Application ALU Using CMC Full Adder with Operational Amplifier is 2.3mW.

B.Delay

Compared to the conventional Mirror Full Adder the Conventional Mirror Full Adder with Operational Amplifier the delay is Reduced up to 52% the delay is 1.85ns. Designing of Application ALU Using CMC Full Adder with Operational Amplifier is 2.48ns

C.Area

Compared to the Conventional Mirror Full Adder the conventional Mirror Full Adder with Operational Amplifier the Area is Decreased upto38% The Area is 166nm.

TABLE I. **PARAMETER CALCULATION FOR CMC FULLADDER AND CMC FULLADDER WITH OPERATIONAL AMPLIFIER**

DESIGN	POWER(mW)	DELAY (ns)	AREA (nm)
CMC FULLADDER	2.6	2.73	2400
CMC FULLADDER WITH OP AMP	1.3	1.29	166
ALU EXISTING METHOD	4.39	3.27	-
ALU PROPOSED METHOD	2.3	2.48	-

Conclusion

Schematic and simulation, layout generation, and an LVS check were used to successfully implement and verify the CMC full-adder with Operational Amplifier design. The entire Design is implemented in Cadence 28nm. Design in Modern integrated circuits can use this architecture since it satisfies the requirements for high-speed operation with energy-efficient features in CMOS technology. In contrast to CMC Full Adder 50% less power, 52% less delay, and 38% less area is used. The procedure used guarantees a strong design that can be effectively produced and included into a more extensive digital system and Also the Application ALU in using CMC Full Adder and CMC Full Adder with Operational Amplifier Both Implementing Arithmetic Functions and

Voltage Level Shifting. Design of ALU Using CMC Full Adder Compared to the ALU Full adder With Operational Amplifier the Power and Delay are reduced.

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