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Implementation of Current Starved Vco in 45nm Cmos Technology

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Abstract

A Voltage Controlled Oscillator (VCO) is a ring oscillator that produces a periodic signal whose frequency is managed by a voltage input. A rising number of applications have necessitated the creation of low-power, high-speed oscillators in recent years. One promising design is the current starved ring oscillator, which controls the amount of current flowing in the inverter stages to regulate the frequency, hence these can be used rather than conventional ring oscillator. Basic principle of a current-starved VCO is using a pair of transistors in a cross-coupled configuration to form a feedback loop that produces a sinusoidal waveform. The voltage delivered to the transistors can be varied in order to change the oscillator's frequency. In this paper a current starved VCO is implemented in 45nm to produce stable frequency. The power, frequency aspects of it are observed and compared.

Keywords: VCO, 45nm, PMOS, NMOS, Current Starved

1. Introduction:

The CMOS VCO (Voltage-Controlled Oscillator) is implemented using complementary metal-oxide-semiconductor (CMOS) technology. It's a popular choice for frequency synthesis in modern electronic systems due to its low power utilization, small size, and high frequency stability. It is commonly used in applications like wireless communication systems, phase-locked loops (PLLs), and frequency modulators. In the recent past, a rising interest is observed in developing low-power and high-speed oscillators for various applications. VCO is a type of ring oscillator whose frequency is controlled by a voltage input. It has odd number of inverting stages to generate a periodic signal. The output signal frequency is calculated by the delay through each stage of the ring oscillator, which can be controlled by adjusting the bias voltage of the transistors in the circuit.

A current-starved VCO is a VCO that operates by controlling the current passing through its core circuitry rather than controlling input voltage. This approach is commonly used in integrated circuits (ICs) for producing oscillations with precise and stable frequencies. The basic principle behind a current-starved VCO involves utilizing a current source to provide a constant current to the core circuitry. By modulating this current, the VCO's output frequency can be adjusted accordingly. The core circuit typically consists of a series of inverters, delay elements, or other suitable integrant to produce the desired oscillating waveform.

To control the oscillation frequency, a control voltage is applied to a control port of the VCO. This control voltage is used to alter the bias current provided by the current source. As the bias current changes, so does the frequency of the oscillating waveform generated by the VCO. One advantage of a current-starved VCO is its ability to offer improved frequency stability and reduced phase noise compared to voltage-controlled VCOs. This is owing to the current in the core circuitry is less susceptible to variations in power supply voltage or temperature changes. Moreover, the use of a current source provides a higher level of control and precision over the oscillation frequencies. Current-starved voltage-controlled oscillators are utilized in a range of applications like frequency synthesizers, phase-locked loops (PLLs), wireless communication systems, and other electronic devices that needs

accurate and stable frequency generation.

In comparison with other VCOs, a current-starved VCO has several advantages:

• Low power consumption: A current-starved VCO utilizes less power than other VCOs because it uses a current-starved topology. That is the oscillator circuit is planned to operate with a limited amount of current, which reduces power consumption.

• High frequency stability: A current-starved VCO has high frequency stability because it uses a differential CMOS transistor to generate the output signal. The differential CMOS transistors provide a high degree of noise immunity, which results in a stable output signal.

• Low phase noise: A current-starved VCO can be designed with low phase noise because it uses differential CMOS transistors to produce the output signal. The differential CMOS transistors provide a high degree of noise immunity, which results in low phase noise.

• Easy integration: Current-starved VCOs are highly conducive to seamless integration into various systems because it uses a standard CMOS process. This means that it can be easily used with other CMOS circuits, which simplifies the designing of complex systems.

• Conventional ring oscillators have some advantages, such as simplicity and ease of implementation, they also have few disadvantages that limit their use in certain applications.

• Limited frequency range: The frequency scale of the oscillator is constrained by the time it takes for signals to propagate through the inverting stages. When the number of stages increase, the propagation delay increases, restricting the highest achievable frequency of the oscillator.

• High power consumption: Ring oscillators consume a relatively high amount of power because they use more number of inverter stages. This could be a disadvantage in applications where power consumption is a critical factor.

• High phase noise: Ring oscillators tend to exhibit elevated phase noise due to the jitter caused by the inverting stages. This can be a drawback in situations that demand minimal phase noise.

• Sensitivity to process variations: Ring oscillators are sensitive to process variations, which might affect the frequency and stability of the output signal. This can be a significant disadvantage in applications where high precision and stability are required.

• Limited tuning range: Ring oscillators have a limited tuning range because they rely on the propagation delay of the inverting stages to generate the output frequency. This limits their ability to generate frequencies over a wide range.

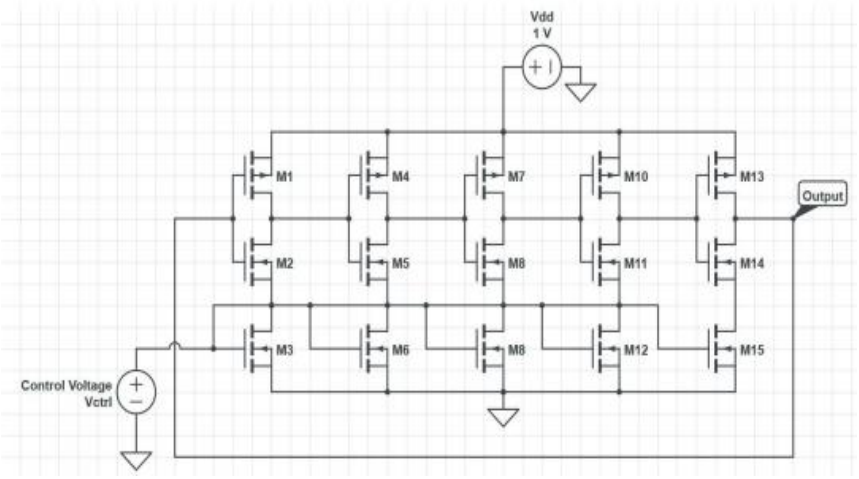

Figure 1: Conventional Ring Oscillator [1]

2. Related Work:

A Voltage Controlled Oscillator (VCO) is an oscillator that can produce a variable output signal within a certain range. [1]. This variation is regulated using an input DC voltage. VCOs are commonly used in applications where simple oscillations are needed, such as bit synchronization, frequency-shift keying, and frequency modulation. The frequency at the output can vary from few hertz to gigahertz, depending on how the VCO is designed. In the context of a Phase Locked Loop (PLL), different types of VCOs, such as Voltage Controlled Ring Oscillators, Current Starved Voltage Controlled Oscillators, and Negative Skewed Oscillators, can be designed with a focus on system performance and layout considerations. Waveforms and parameters are compared to achieve high performance, and layouts are designed with the goal of maximizing the area under high priority. Layout verification is performed using tools like Design Rule Check and Layout vs. Schematic Assura quality checks. All the designs mentioned are implemented using the 45nm technology node and the gpdk45 technology in the Cadence Virtuoso System Design Platform.

The second paper presents a five-stage CMOS Ring Voltage Controlled Oscillator (RVCO) technique for low-power Phase Locked Loop (PLL) applications [2]. The RVCO with frequency of 3.22 GHz and is designed using a 45nm CMOS technology with various threshold voltage values. To enhance the switching performance of MOSFETs, a current-starved power switching technique is utilized. The CMOS circuit demonstrates excellent linearity in a tuning range from 900 MHz to 3.22 GHz, with control voltage range spanning from 0.6V to 1V. The RVCO exhibits a phase noise level of -71.9 dB at a 1 MHz of offset frequency. At control voltage of 0.6V, the circuit consumes a power loss of 4.18 uW. The RVCO, designed using a low-power CMOS approach and the current starved technique with a parallel-connected transistor in 45nm technology, has been simulated using the Cadence Virtuoso tool. The RVCO exhibits a phase noise level of -71.9 dB at a 1 MHz offset frequency. Furthermore, when control voltage is set at 0.6V, the circuit consumes a power dissipation of 4.18 uW. The RVCO operates and is analyzed within the controlled voltage range of 0.6V to 1V. Simulation is done in the Cadence Virtuoso tool. The RVCO design operates in the five-stage power switching mode, reaching frequency of 3.22 GHz. It consumes a power dissipation of 0.1 mW and exhibits a phase noise level of -71.9 dB at a 1 MHz offset frequency.

Oscillators play a crucial role in both analog and digital circuits, finding extensive usage in communication and electronics systems. They are fundamental devices that generate continuous periodic signals and serve various purposes such as signal synthesizers, clock generators, phase-locked loops, and regenerative repeaters. The mentioned paper [2] focuses on designing a single-ended CSRO as a clock for a System-on-Chip (SoC). The circuit is designed to be low power, independent of process and temperature, and implemented using Cadence Virtuoso in TSMC 180 nm technology. It achieves a stable oscillation frequency of 1 MHz, making it suitable for SoC applications. The oscillator consumes 0.075 mW of power at normal temperature with a VDD of 1.8 V. To account for power supply variations, the oscillator is driven by a Low Dropout (LDO) regulator. To address temperature variations, a temperature compensation circuit is incorporated to reduce frequency variations across different temperatures. The frequency variation observed across a temperature range of -40°C to 125°C is within ±2.5%. Additionally, trim bits are incorporated to regulate the frequency across different process corners. As a result, an overall frequency variation of ±3.5% is achieved.

Switched capacitor circuits (SC) have gained widespread usage in various signal processing blocks like filters and ADCs due to its advantages of lower power utilizes and smaller area. To implement switch capacitor circuits, a nonoverlapping clock and an oscillator are necessary. In mentioned paper [3], a novel inverter is proposed specifically for designing a low-power and frequency clock generator oscillator. The proposed inverter configuration comprises a series of cascaded current-starved inverters and a current-starved inverter connected in an inverted manner. Using Cadence Virtuoso simulation with GPDK 90nm, the designed inverter block demonstrates a delay of 866 ps, which is approximately 40% longer than that of the conventional design. The implemented oscillator achieves the0 frequency of 51 MHz and consumes a power of 100.6 µW, which is thrice lower than the conventional design's power consumption.

In the domain of analog/mixed-signal design has recently been emphasizing the design of low-power, high-speed

designs to cater to portable applications like IoT. Paper [4] introduces an inverter configuration that intentionally introduces a longer delay while operating at low power. This inverter design proves useful in creating a low-power and low-frequency ring oscillator, which can serve as a clock generator in IoT applications. The proposed inverter is composed of two stages interconnected in a cascade arrangement. The design is simulated using Cadence tool in 180nm technology. Simulation results showcase a delay of 10.9 ns for the proposed inverter, which is 143.3% longer than that of the conventional design. Additionally, the implemented oscillator achieves a frequency of 17 MHz while consuming a power of 144.75 µW. These characteristics make it suitable for potential IoT applications and RFID tagging operations ranging from 12 MHz to 1 GHz.

Paper [5] presents a offer a analysis of a three-stage MOS capacitance-based current starved ring voltage-controlled oscillator (VCO). The VCO operates by adjusting the frequency through the variation of MOS transistor capacitance using a variable tuning voltage. To achieve a current-starved condition, a current source is implemented using a PMOS current mirror technique. The designed and implemented VCO follows a 90nm CMOS process technology. Simulations are conducted with a 1V supply voltage, while the controlling voltage ranges from 0V to 0.6V. The results demonstrate that the MOS capacitance-based current starved design offers better tuning range of 4.22 to 6.22 GHz, accompanied by low power consumption of approximately 0.368 mW. The figure-of-merit is measured at -155.3 dB/Hz and a phase noise of -77.87 dB/Hz at a 1 MHz offset. This VCO design holds potential for utilization in wireless applications such as IEEE 802.11a.

Paper [6] conducts a comparative analysis of two different architectures, namely CMOS and NMOS Ring Oscillators, as well as a current starved Voltage-Controlled Oscillator (CS-VCO). The study focuses on evaluating their performance parameters, including power utilisation, phase noise, and output swing. The designs are implemented using a 180-nm CMOS technology node, and a center frequency of 2.5 GHz is selected for comparison due to its relevance in Wi-Fi and Bluetooth applications. The comparative study provides an intuitive understanding of the performance parameters mentioned. The data reveals that the NMOS-based Ring Oscillator exhibits the best Phase Noise performance of -72.94 dB/Hz at a 1 MHz offset frequency from the 2.5 GHz center frequency. Conversely, the CMOS Ring Oscillator demonstrates the most favorable power consumption, consuming merely 4.61 µW.

In paper [7], two innovative voltage-controlled oscillators (VCOs) based on transmission gates, namely TG-I VCO and TG-N VCO, are introduced. Both VCO designs employ a total of 26 transistors. The TG-I VCO operates within a frequency range of 18.965 MHz to 1.925 GHz, while the TG-N VCO covers a broader range from 4.5 MHz to 4.28 GHz. The tuning ranges for TG-I VCO and TG-N VCO are observed to be 99.015% and 99.89% respectively. Additionally, the achieved gain values are 14.2 Grad V−1 for TG-I VCO and 17.5 Grad V−1 for TG-N VCO. Through phase noise analyses, it is obtained that the TG-I VCO exhibits a phase noise response of -135.42 dB/Hz at 1 MHz offset frequency, while the TG-N VCO demonstrates a phase noise response of -127.29 dB/Hz at the same offset frequency. The circuit designs were implemented in the Cadence Virtuoso Environment and utilized the GPDK 180nm library of CMOS technology, operating at a VDD of 1.8 V.

In a research paper [8], a high-frequency, low-power current-starved sleep voltage-controlled oscillator (VCO) is introduced. Among different oscillators, the current-starved VCO is popular due to its compact size broad spectrum. The power utilization of the VCO significantly affects the overall performance of low-power PLLs. To address this issue, various inverter delay approaches can be in order to decrease leakage power. These approaches involve introducing a sleep transistor in-between the pull-up MOSFET and the VDD of the inverter, hence reverse biasing it such that it reduces the leakage current in sub-threshold region when both transistors are turned off. The current-starved sleep VCO is realized using CMOS 90nm technology and is evaluated at an operational frequency of 1 GHz, offering a tuning scale from 0.5 GHz to 5.8 GHz. Notably, the power loss of the VCO is measured at 8.12uW, which is approximately 2.3 times lower than that of a conventional VCO.

In paper [9], a comparative study is conducted on two different ring oscillator architectures (CMOS and NMOS) and a current-starved voltage-controlled oscillator (CS-VCO). The study focuses on numerous parameters such as power dissipation, phase noise, etc. All designs are realized using 45-nm CMOS technology, and a center frequency of 2.3 GHz is chosen for comparison due to its relevance in AV devices and radio control applications.

By performing a comparative analysis, the study provides insights into the performance characteristics of each oscillator architecture. The data reveals that the NMOS-based ring oscillator exhibits superior performance. Specifically, the NMOS ring oscillator achieves a phase noise level of -97.94 dB/Hz at a 1 MHz of offset frequency from the 2.3 GHz center frequency. Conversely, the data also demonstrates that the CMOS ring oscillator is favorable with respect to power consumption. The CMOS ring oscillator consumes only 1.73 mW of power, which is relatively low compared to other options. Overall, the comparative study sheds light on the trade-offs between different oscillator architectures, highlighting the strengths of the NMOS ring oscillator in terms of phase noise performance and the CMOS ring oscillator with respect to power consumption.

3. Proposed Work:

The proposed design of current starved ring oscillator is for low power devices, this can be achieved by reducing the current which further reduces the power. The VCCS is typically implemented using a differential CMOS transistor biased by a constant current source. The input voltage is applied to the gate of one of the transistors, which modulates the current passing through the differential pair. Each PMOS and NMOS are connected serially as the current starved transistors to the inverter PMOS and NMOS transistors respectively and the respective power lines at each transistor. And a pair of NMOS and PMOS form the biasing circuit. Here, the current starved VCO is designed to have 5 stages. The oscillation frequency depends on delay introduced by each stage. Frequency of oscillation is observed as inverse of number of stages and also time taken to charge and discharge the capacitance present in between stages, as shown in equation 1

$$f0 = \frac{1}{2N\tau d} \qquad \ldots\ldots(1)$$

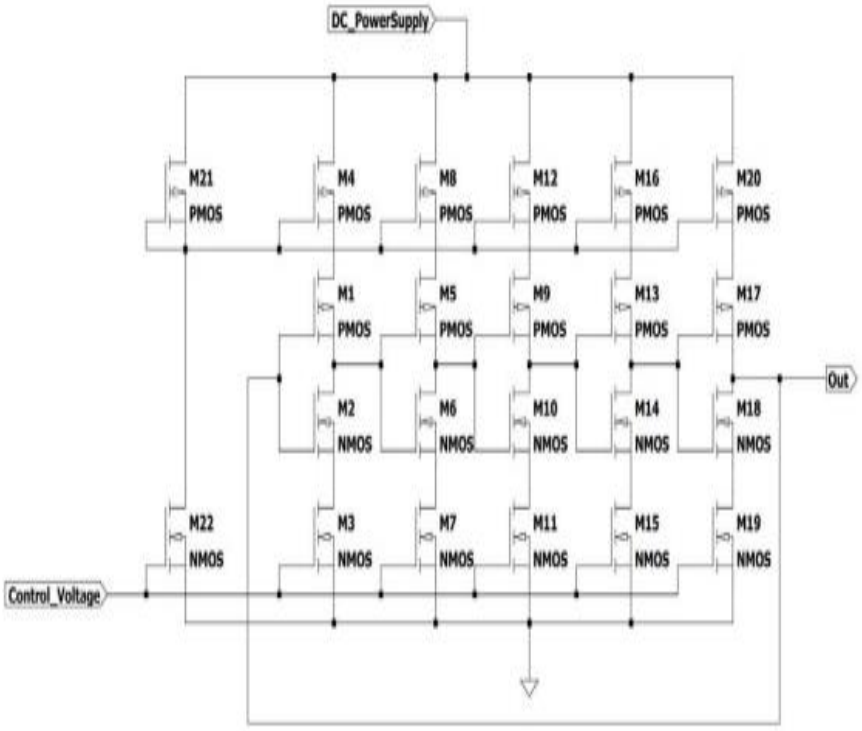

Figure 2: Proposed 5-stage Current Starved VCO

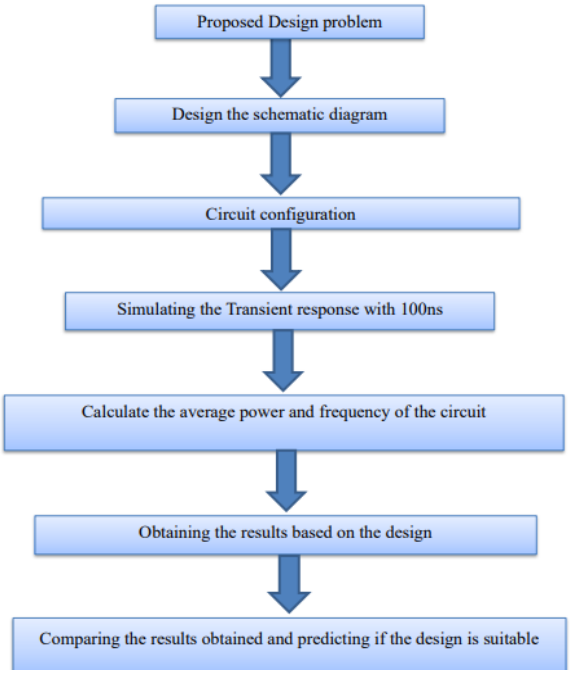

Figure 3: Flow of the proposed methodology

4. Results and discussion:

The current-starved voltage-controlled oscillator (VCO) is implemented in 45nm technology with VDD of 1.2V. It is designed for 5 stages and stable oscillations is at the output with frequency of 2.7 GHz and the power consumed is 53.48uW. The feedback path is initialized to zero and hence the output of each inverter stages is observed.

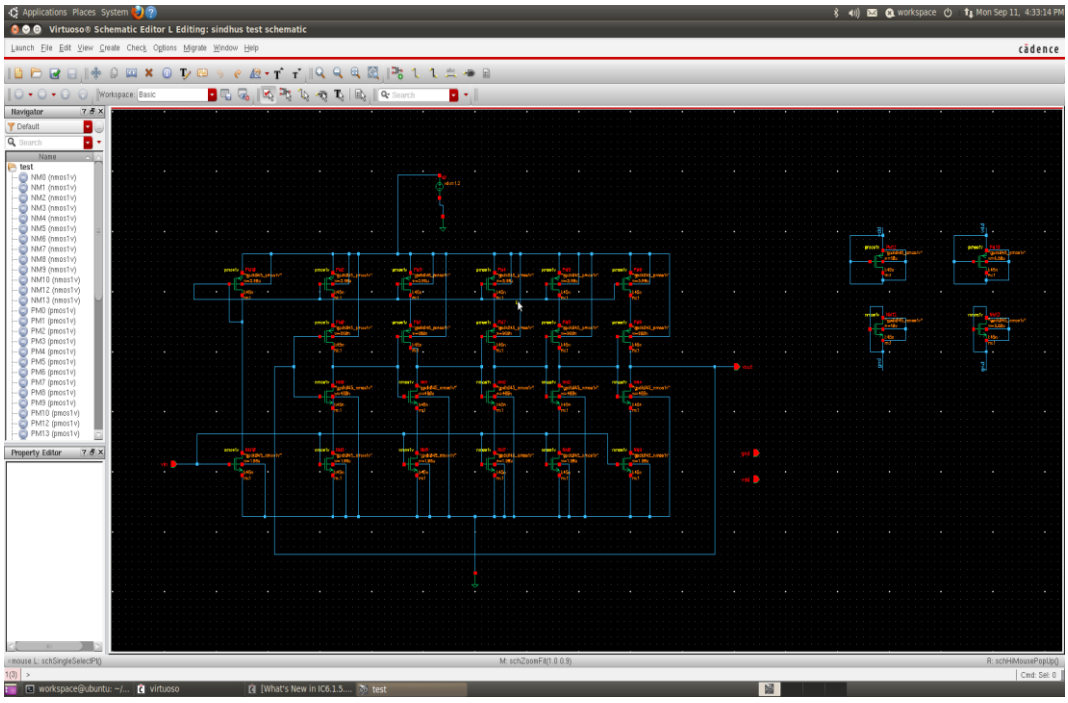

Figure 4: Schematic of proposed Current Starved VCO

Table 1: Comparison of the obtained results

Parameter	Conventional Ring VCO	Current starved VCO	Paper [2]
Power supply	1.2V	1.2V	1V
Frequency	3.27GHz	2.7GHz	3.22GHz
Power consumption	0.6mW	53.48uW	0.1mW

OUTPUT WAVEFORMS

The graph obtained through transient analysis of the output node is shown in fig 5. It depicts the stable oscillations of the current starved VCO.

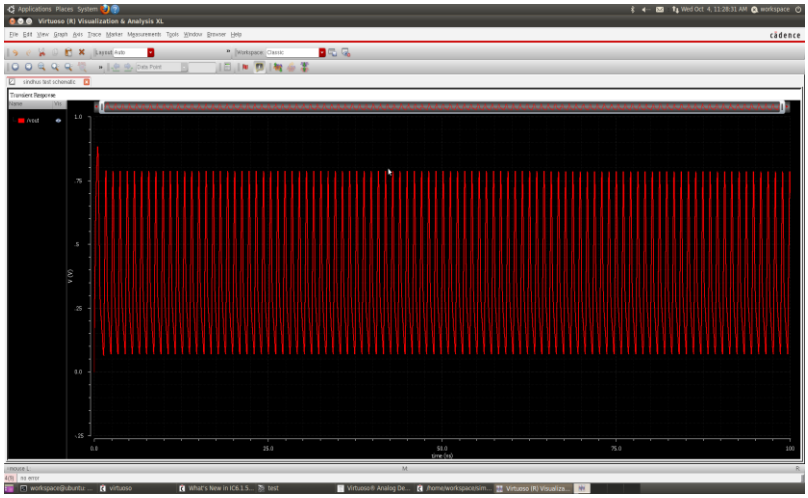

Figure 5: Transient response of the circuit

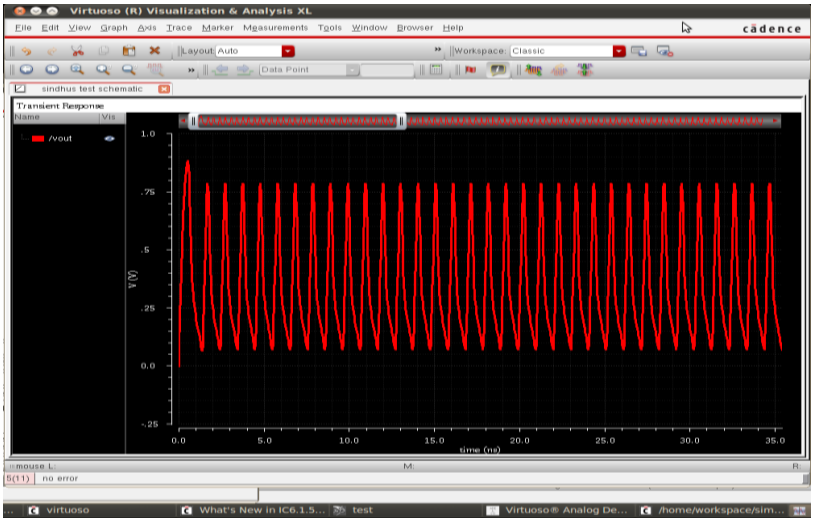

Figure 6: Closer view of the transient response obtained

The fig 7 depicts the transient response of each inverter stage which shows that the output of one stage acts as input to the next stage where it is further being inverted. This oscillation continues to the output of the VCO

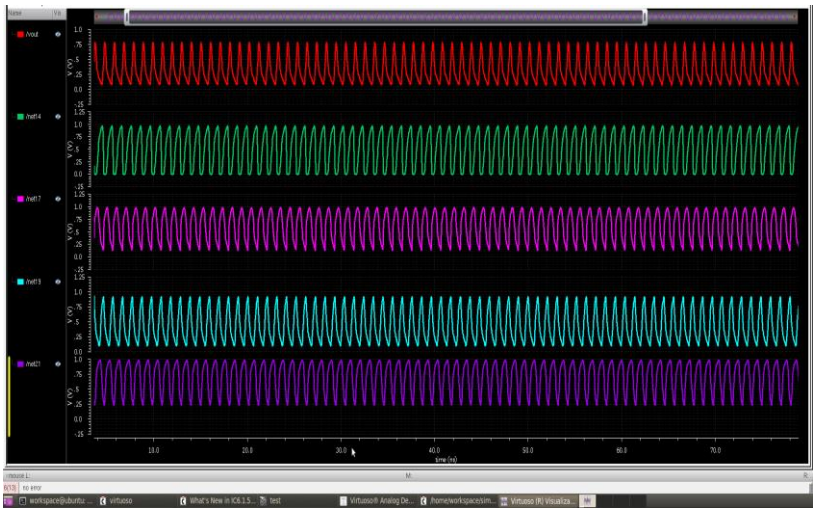

Figure 7: Transient response of each inverter stage

The average power at the output of the circuit is obtained by considering the overall power ranges from the graph and taking the average of it. The graph corresponding to the different values of power at different duration of time is shown in fig 8

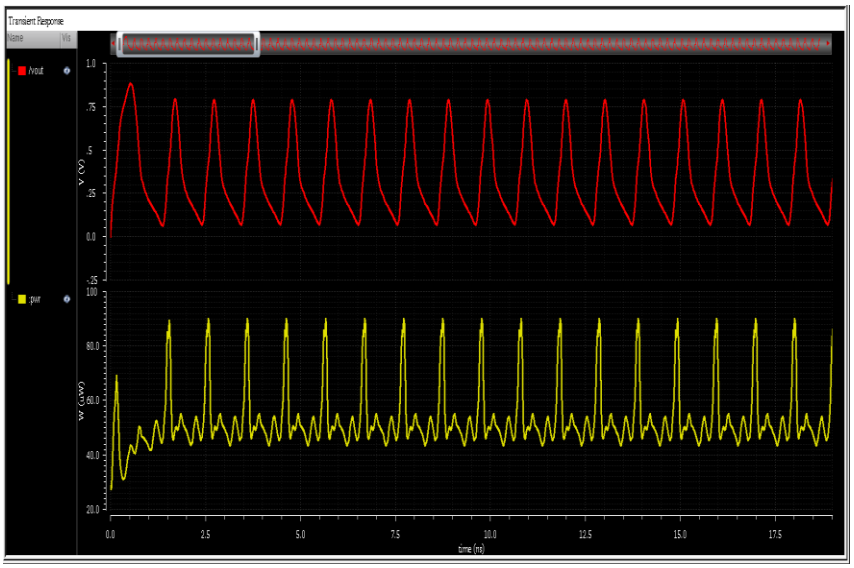

Figure 8: Graph obtained for power analysis

5. Conclusion

The current-starved voltage-controlled oscillator (VCO) is a widely used circuit in modern electronics due to its simplicity, efficiency, and stability. This work mainly focuses on designing of Current Starved VCO. The proposed methodology provides optimization to various parameters of VCO such as delay, power stability of oscillations thereby increasing the efficiency when compared with the ring VCO or any other CMOS VCO design.

The circuit consists of a voltage-controlled current source and a resonant tank circuit, which work together to produce a periodic output such that its frequency is controlled by an input voltage. The current-starved VCO is called so because the current flowing through the MOSFETs is intentionally limited to a small value, which reduces power consumption and improves the linearity of the output frequency. This makes it a better choice for

devices that require a stable and tunable oscillator, such as frequency synthesizers and phase-locked loops. Overall, the current-starved VCO is a valuable contribution to the field of electronics. Due to these facts, this design is most extensively used for research purposes to observe oscillator behavior when transistors are scaled and are implemented for widespread applications, mainly FinFET.

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