Tuijin Jishu/Journal of Propulsion Technology
ISSN: 1001-4055
Vol. 45 No. 3 (2024)

High Speed Ternary Content Addressable Memory for Network Applications Using Transmission Gate Logic

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Abstract;

Ternary Content Addressable Memory (TCAM) is a critical component in modern network systems, widely used for high-speed packet transmission and classification tasks in routing tables because of its superior lookup speed. However, the substantial number of transistors used for its operation results in noteworthy power utilization and delay. This paper explore traditional TCAM designs alongside advancements aimed at improving performance, reducing power utilization, and improving searching speed. Leveraging power gating and Transmission Gate Logic (TGL), the proposed TCAM architecture enhances energy efficiency while ensuring data security. The proposed architecture aims at reducing dynamic along with leakage power. The work is carried out in cadence virtuoso 45nm and the result has shown that there is significant reduction in delay and bearable power consumption. The delay is observed to be 56.7ps and the overall power consumption of 92.91uW. The results when compared with the architecture used in previous work shows significant improvement in delay that is, up to 84%, with a sustainable increase in power utilization to about 13%.

***Keywords*:** Addressable Memory, Transmission Gate Logic

1. Introduction:

Utilizing a range of technologies, such as radio, optical, satellite, and wireless networks, information is transferred over long distances via telecommunication. Communication speed is a measure of how fast data can be sent and received over a communication channel, and it's usually expressed in bits per second (bps). Communication speed is important for telecommunication applications, as it affects the quality,reliability, and efficacy of the information exchange. For fast and efficient data transfer to happen we need resourceful routers, that enables easy and quick data search operations.

Content-addressable memory (CAM) is a type of memory that allows fast searching of data based on its content, rather than its address. CAM can help improve communication speed in telecommunication applications, as it can perform parallel search operations in one clock cycle, reducing the time and energy required for data lookup and retrieval. Additionally, CAM can provide approximate matching, which allows for a tolerance of a specific Hamming distance (number of mismatched bits) between a query pattern and the stored data. This can make data processing faster and more versatile, especially for applications like image identification, natural language processing, and genomics that deal with noisy, partial, or ambiguous data. Because CAM may use encryption and authentication techniques based on the substance of the data rather than its location or address, it can also improve the security and privacy of communication.

Content-Addressable Memory (CAM) is a specialized type of computer memory that allows for parallel search and retrieval of information based on content, rather than requiring an address. Unlike traditional memory, where data is accessed by providing a specific memory address, CAM allows for direct matching of data content. This feature makes CAM particularly useful in applications where rapid searching and retrieval basedon content are essential. CAM is commonly employed in networking devices, such as routers and switches, tofacilitate fast and efficient packet routing.

There are various types of CAM, depending on how the data and the tags are stockpiled and compared. Some of the common types of CAM are:

i. Binary CAM (BCAM): It is the simplest type of CAM, where each data word is saved with a binary tag that uniquely identifies it. The search operation compares the input tag with all the stored tags in parallel andreturns the matching data word and its address. BCAM is fast and easy to implement, but it uses a large amount of memory space to store the tags and data.

ii. Ternary CAM (TCAM): It is a more flexible type of CAM, where each data word is saved with a ternarytag that can have three values: 0, 1, or X (don't care). The search operation compares the input tag with all the stored tags in parallel and returns the matching data word and its address. TCAM allows for partial or wildcard matching, which is useful for applications such as routing tables and packet classification. TCAM is more complex and expensive than BCAM, but it requires less memory space to store the tags and data.

iii. Quaternary CAM (QCAM): It is a type of CAM that uses four values: 0, 1, 2, or 3, to store the tags and data. QCAM can store added information per bit than BCAM or TCAM and can also support partial or wildcard matching. QCAM is more difficult to implement and consumes more power than BCAM or TCAM,but it can decrease the memory size and improve the search performance.

iv. Fully associative CAM (FACAM): It is a type of CAM that does not utilize any tags to save the data. Instead, the search operation compares the input data with each and every stored data in parallel and returns the address of thematching data word. FACAM can store any type of data and does not use any encoding or decoding, butit is very slow and inefficient compared to other CAMs.

In network packet routing, Ternary Content-Addressable Memory (TCAM) holds significant importance. TCAM is specifically designed to handle more complex matching conditions, making it well-suited for tasks like IP address lookup and access control list (ACL) matching. TCAM's ability to perform rapid and parallel searches built on numerous matching criteria, including exact matches and wildcard matches, is crucial in efficiently determining the next hop for a packet in a network. This flexibility in matching conditions is particularly valuablein scenarios where routing decisions are grounded on a combination of source and destination addresses, protocoltypes, and other attributes. The use of TCAM in networking devices contributes to high-speed and low-latency packet processing, ensuring that data is swiftly and accurately directed through complex network paths. Overall,TCAM enhances the speed and efficiency of network packet routing by providing advanced and flexible content-based matching capabilities. While TCAM's parallel search mechanism offers low latency, it also results in highpower consumption due to the huge number of transistors involved. Each TCAM cell typically consists of several transistors, significantly more than a standard SRAM cell, which might use only 6 transistors. The high transistor count arises from the need to store ternary data (0, 1, X) and perform rapid parallel comparisons.

2. Related Work:

The data retention based TCAM (DR-TCAM) technique significantly reduces leakage power in TCAM memory by dynamically adjusting the power source of mask cells without destroying mask data. Simulation results demonstrate that DR-TCAM achieves a 41% reduction in TCAM leakage power and a 12% reduction in total power, with only a 1.1% loss in search performance. This technique outperforms traditional designs and related methods by maintaining data integrity even in standby mode while delivering superior power reduction and search efficiency. [1]

Three components make up a TCAM cell: an SRAM cell, evaluation logic, and an XOR-type CAM cell. The data (D) that will be compared with the search data (SL and SLB) is stored in the XOR-type CAM cell. The mask data (M), which indicates whether this TCAM cell is the "X" state (i.e., don't care) is stored in the SRAM cell.The compare result needs to match when the TCAM cell is the "X" state. The network router's job is to forward incoming packets to other routers in accordance with the packet header's destination IP address.

In Figure 1, a typical TCAM cell consists of three main components. The first is an 8T XOR-type cell, which compares the stored data with the input search data. The second component stores the mask bit, which indicates if the TCAM cell is in the "don't care" (X) state. The third component includes logic built with two nMOS

transistors in series, controlled by the mask bit and the XOR result from the CAM cell, determining the search result based on whether the Match Line (ML) is pulled down or not. The differential search lines (SL and SLB) and differential bit lines (BL and BLB) are two pairs of lines used for search and read/write operations. During standby mode, the ML is kept at a pre-charge voltage, and the SL and SLB are held at 0. After pre-charging, search operations proceed with search data set on SL and SLB.

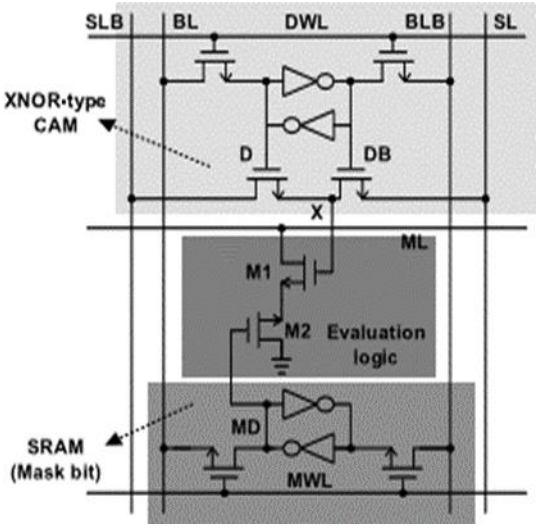

Figure 1: Traditional TCAM [1].

Several operations corresponding to the input nature is described as follows (summarized in Table I). In Search 1 operation, when cell data are 1, the ML is kept near precharge voltage (match). In contrast, if cell data are 0, the result of the CAM cell (X) exceeds the threshold voltage of M1 to enable M1, and ML is pulled down to ground (mismatch). The Search 0 operation is similar, but if the mask bit is 0, irrespective of whether the result of the CAM cell is match or mismatch.

Operation	Data	Mask	V_{ML}	Result
Search 1 (SL=1, SLB=0)	0	1	Low	Mismatch
	1	1	High	Match
	0	0	High	Match
	1	0	High	Match
Search 0 (SL=0, SLB=1)	0	1	High	Match
	1	1	Low	Mismatch
	0	0	High	Match
	1	0	High	Match

Table 1: Three kinds of mask segments [1]

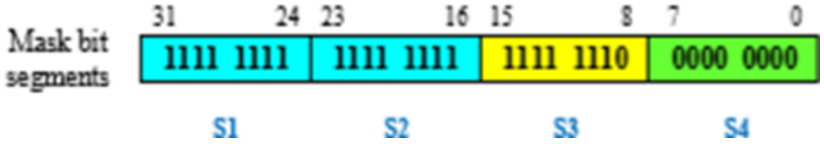

Figure 2: Example

Mask Data segment	Meaning	Example in Fig. 2
1...1...1	All 1s	S1 and S2
1...10...0	Boundary segment	S3
0...0...0	All 0s	S4

Table 2: Segments description [1]

This study introduces a 32nm technology-based TCAM using Carbon Nanotube FETs (CNTFETs) as a superior alternative to MOSFETs. Simulations using VS-CNTFET and S-CNTFET models reveal a substantial reduction in the Power-Delay Product (PDP) compared to MOSFET counterparts, with the VS-CNTFET TCAM array achieving up to 27.53% lower PDP than MOSFET-LP. The results indicate that CNTFET-based TCAMs provide the best performance, and the study suggests extending the research to larger TCAM arrays for further evaluation. [2]

The paper introduces a novel TCAM design utilizing a 2T2R RRAM array with a current-race sensing mechanism and match-line booster to enhance energy efficiency, search speed, and variation tolerance. Innovations such as match-line sensing amplifier direct cascading, SR-latch cascading schemes, and an RRAM-based tunable delay element contribute to improved performance and robustness. The proposed 64-bit 1-stage TCAM demonstrates exceptional speed and energy efficiency, outperforming other eNVM and SRAM-based TCAM designs, making it ideal for large-scale memory applications like network routers, image processing, and neural network acceleration. [3]

The work proposes an innovative 11T SRAM cell capable of functioning in four modes—SRAM, logic, BCAM, and TCAM—with both column-wise and row-wise operations. It achieves a frequency of 595MHz and an energy consumption of 17.94fJ/bit in logic mode, and in BCAM/TCAM modes, it operates at 407MHz with energy consumption of 0.62fJ/bit and 1.38fJ/bit, respectively. This design, using TSMC 65nm technology, features column access ports and decoupled read/compute ports, making it highly versatile for various in-memory computing applications. [4]

The paper introduces a DMTJ-based NV-TCAM design that uses a voltage divider structure and dynamic-logic sensing network, significantly reducing write and search energy by 73% and 79% respectively, and lowering the search error rate by 3.8 times compared to previous designs. Despite increasing search time, the design maintains sub-nanosecond performance and achieves a 4× smaller cell area, making it highly efficient and compact. This NV-TCAM, designed using the 28 nm FDSOI process, is particularly suited for associative processor applications such as in-memory deep learning processors, where both write and compare operations are frequent.[5]

The paper presents a high-speed, energy-efficient single-port (SP) CAM design that achieves dual-port (DP) operation in superscalar processors through two novel peripheral schemes, CShare and VClamp. These schemes significantly reduce search delay by approximately 87% and improve energy efficiency by about 85% compared to state-of-the-art CAM designs, demonstrating a 45.6% average energy efficiency improvement over traditional DP CAM. The study, verified through various conditions and Monte-Carlo simulations, marks the first demonstration of DP CAM operation with an SP CAM structure and plans to explore post-layout simulations and parasitic effects in future work. [6]

The paper introduces two TCAM architectures that significantly reduce power consumption by using low-power 6-T and 8-T SRAM cells, with the designs tested and simulated using Cadence Virtuoso and gpdk090 technology. The low-power 8-T TCAM achieves a 67% reduction in power consumption, while the single-ended 6-T TCAM achieves a 17% reduction, both maintaining optimal static noise margins (SNM) across extreme temperatures. These improvements make the proposed TCAM architectures highly efficient and adaptable for various low-power applications. [7]

The paper introduces novel memristor-based CAM architectures optimized for reduced power consumption,

compact physical layout, and performance simplicity, offering more attractive options for future manufacturing. These architectures for binary and ternary CAM cells achieve lower power use, fewer active elements, and streamlined single-step writing and searching operations. The improvements were validated through simulations under consistent parameters and conditions for all cells. [8]

The article presents an ultra-high-speed memristor-based TCAM (MTCAM) designed for real-time and big-data applications, offering low power dissipation and rapid data retrieval. The proposed MTCAM cell utilizes memristors for bit storage and an ultra-fast match line sense amplifier, achieving a 1.12 times faster search speed and 67% less search energy per bit compared to the fastest existing design, according to SPICE simulations on 45 nm technology. The simulation results indicate a search delay of 175 ps, a sense margin of 195 mV, and an average search energy consumption of 1.2 fJ per bit. [9]

The study introduces a magnetic skyrmion-based ternary CAM (Sky-TCAM) cell with a 5T2R structure, designed for high-speed search applications like network routers and machine learning. Sky-TCAM utilizes XOR logic through the polarity of search currents and stored bits, and a mismatch discharges the matchline by placing a skyrmion beneath one of the MTJs, leading to efficient operation. The design achieves the lowest Energy-Delay Product (EDP) of 8.74×10^{-25} J·s among non-volatile TCAMs, showcasing spintronics as a promising technology for compact, low-power, and low-latency electronic devices. [10]

Paper 11 explores low-power and high-speed Content-Addressable Memory (CAM) designs that perform parallel search operations by comparing search data with stored contents in a single cycle. Using a 65-nm manufacturing node at 1.2V, the study proposes CAM structures that improve upon traditional designs by achieving a 21% faster matching speed and reducing leakage power by 23%. These advancements are validated through comparisons of power consumption, leakage, propagation delay, and area, demonstrating superior performance in speed, efficiency, and compactness compared to traditional precharge-free CAM designs. [11]

Paper 12 introduces a 28-nm nonvolatile ternary content addressable memory (nvTCAM) based on resistive memory (ReRAM) designed to address the high-density and power challenges of TCAM in 5G network applications. The proposed 2-diode-2-ReRAM (2D2R) nvTCAM cell with crossbar array configuration achieves nearly a threefold increase in storage density and supports 3-D stacking for further density improvements. Utilizing machine learning techniques like K-means clustering optimizes search efficiency by focusing on specific memory banks, reducing search energy by over 70% with minimal silicon area overhead. These innovations aim to enhance the speed and efficiency of packet forwarding in 5G routers while ensuring the reliability and durability required for continuous operation. [12]

Paper 13 introduces COLA, a framework designed to enhance the efficiency of TCAM updates in switches used for software-defined networking. By employing a Modified-Entry-First (MEF) write-back strategy and a layered TCAM structure, COLA ensures consistent forwarding behavior during updates. It reduces TCAM movements by up to 88% compared to existing methods, particularly in scenarios involving rule reordering, demonstrating substantial improvements in update efficiency and forwarding consistency. [13]

Paper 14 introduces a novel 2T2R ReRAM structure designed to tackle latency and power consumption challenges in big-data and machine learning applications. This architecture supports TCAM functionality, logic in-memory operations, and in-memory dot product computations for Deep Neural Networks (DNNs), alongside conventional non-volatile memory functions. The design features reconfigurable sense amplifiers and split word-line drivers, enabling high-density storage and efficient operation as a versatile accelerator for data-intensive tasks, particularly suited for edge devices requiring low-latency and energy efficiency. [14]

Paper 15 introduces a novel TCAM architecture using Nanoelectromechanical (NEM) Memory Switches for nonvolatile data storage, aimed at reducing power consumption and improving chip density compared to traditional CMOS-based designs. The TCAM word array, constructed with 10-bit cells based on NEM Memory Switches, operates at 1.2V in a 65-nm commercial process. Layout design and verification using Cadence Virtuoso and Spectre simulations demonstrate the feasibility of achieving lower power consumption and potentially compact 3D integration benefits with NEM Memory Switch circuits positioned above CMOS logic layers. [15]

Paper 16 introduces a novel CAM architecture for network routers that achieves substantial energy efficiency improvements. The design, implemented using CMOS 45nm technology with a 1V supply voltage, incorporates a charge control unit to optimize the division of the Match Line (ML) based on specific search requirements, reducing the need for comparison operations by 57% in energy metrics compared to traditional designs. Monte Carlo simulations demonstrate consistent performance superiority across various scenarios, highlighting the potential of this approach to enhance energy efficiency and performance in high-speed table lookup operations. [16]

Paper 17 provides a comprehensive survey of CAM design methodologies and performance enhancements, focusing on approaches like Hybrid Memristor-CMOS, NOR type TCAM, Pseudo nMOS Cell, Master-Slave Match Line (MSML), BiCAM, and DG SB-CNTFET. The study highlights that CAM designs emphasizing low power consumption and high speed are more efficient than traditional models across various applications, including pattern recognition, data compression, and network security. These advancements suggest that future VLSI circuits could benefit from CAM cells featuring compact, high-speed, and energy-efficient memory architectures. [17]

Paper 18 focuses on improving the efficiency of an 8x8 CAM array using Transmission Gate (TG) based CAM cells to reduce power consumption and delay. The proposed design integrates an 8x8 SRAM array, Decoder, Priority Encoder, and Multiplexer alongside the TG CAM cells. Simulation results from Cadence Spectre show that the system achieves a delay of 10.17ns and consumes an average power of 856.05uWatt, demonstrating promising improvements in both performance metrics compared to traditional CAM designs.[18]

Paper 19 introduces DyLAN, a novel approach to dynamic Multi-Level Ternary Content Addressable Memories (ML-TCAMs) using 4-terminal nanoelectromechanical (NEM) relays. DyLAN-W and DyLAN-S variants are proposed to optimize retention time and refresh overhead respectively, achieving significant area reductions of up to 2.7x compared to SRAM-based ML-TCAMs and 4.9x compared to charge-domain ML-TCAMs. The study highlights DyLAN's capability to enhance few-shot learning accuracy by 13.7% on average compared to existing nonvolatile ML-TCAMs, emphasizing its potential for high-density and high-accuracy applications in computational memory. [19]

The results from paper 20 indicate that the power consumption of a 64-bit CAM in the open-source environment closely matches that in the Cadence environment, demonstrating consistent performance across platforms. This consistency suggests that open-source EDA tools can effectively simulate and validate CAM designs without significant discrepancies in power metrics compared to proprietary tools like Cadence. The analysis underscores the viability of open-source tools for assessing CAM performance, particularly in terms of power consumption, which is critical for low-power IC design in portable devices. [20]

3. Proposed Work:

In single clock cycle, TCAMs search the data (IP address). TCAMs are especially desirable for packet transmitting and segregation due to this feature. Rather of employing an 8T XOR-type cell, an additional circuitry is incorporated in 8T XOR type cells to protect the data contained in TCAM. A modified 8T XOR type cell using a two-phase write operation—which consists of equalization and write phases is proposed to address the 8T XOR type CAM cell's information leakage duringwrite operations. This consequences in a significantly lower correlation between the cell's current dissipationand the data it stores. During the equalization stage of the write process, power gating (PG) is utilized ʊ prevent short-circuit power dissipation by turning off the supply voltage of a complete memory word (VVDD). During the equalization stage, transistor PPC is added to the original 6T SRAM architecture to short Q and QB.

By employing a PC signal, PG is turned off and PPC can use charge-sharing to achieve voltage equalization between Q and QB, preventing the supply from using any more power. To finish the write process, PC is discharged in the next phase of the write operation to charge VVDD, turn off PPC, and enable the NMOS access transistors (NA1 andNA2). This allows them to send the data from BL and BLB to Q and QB, respectively.

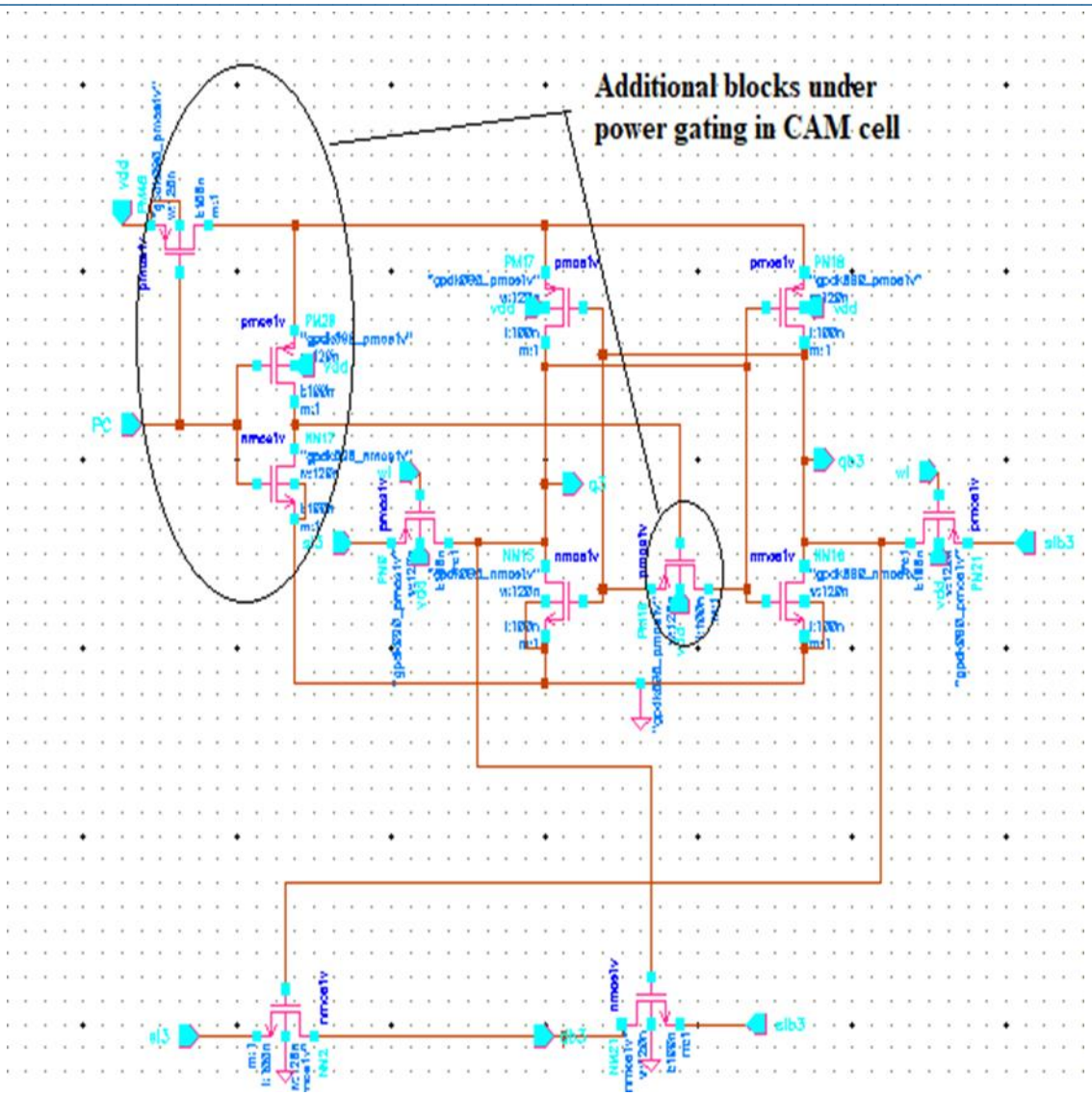

Figure 3: Power gating cells to reduce the overall power consumption.

The transmission gate is a bilateral switch consisting of NMOS and PMOS transistors controlled by externally applied logic levels. Transmission gates act like voltage-controlled switches, and being switches, transmission gates can be used for switching both analogue and digital signals passing the full range of voltages (from 0V to V_{DD}) in either direction, which as discussed is not possible with a single MOS device.

By using this kind of XOR Type cell, the data cannot be attacked and will be secured. Data security is the prime concern of the day since the there is a chance of hacking data which is undesirable. Figure 6 shows the proposed TCAM architecture for 1-bit which makes use of power gating and transmission gatesfor improving the overall performance. The analysis is performed on 4-bit TCAM.

Figure 8 illustrates the operation of a 1-bit TCAM output, where the match line (ml) signal becomes high if both the bit line (bl) and search line (sl) match. This comparison occurs only when both the word line (wl) and the match word line (mwl) are low. These lines are connected to PMOS access transistors that activate when their signals are low. If either wl or mwl is not low, the data is masked (represented as 'x'), and ml enters a ternary state, which reduces unnecessary power consumption.

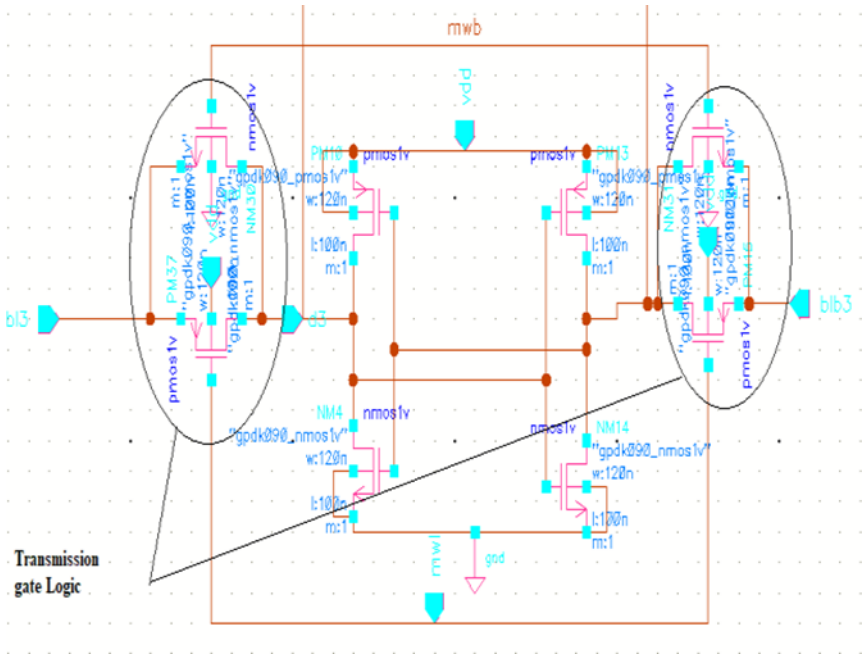

Figure 4: Transmission gates incorporation to overcome delay

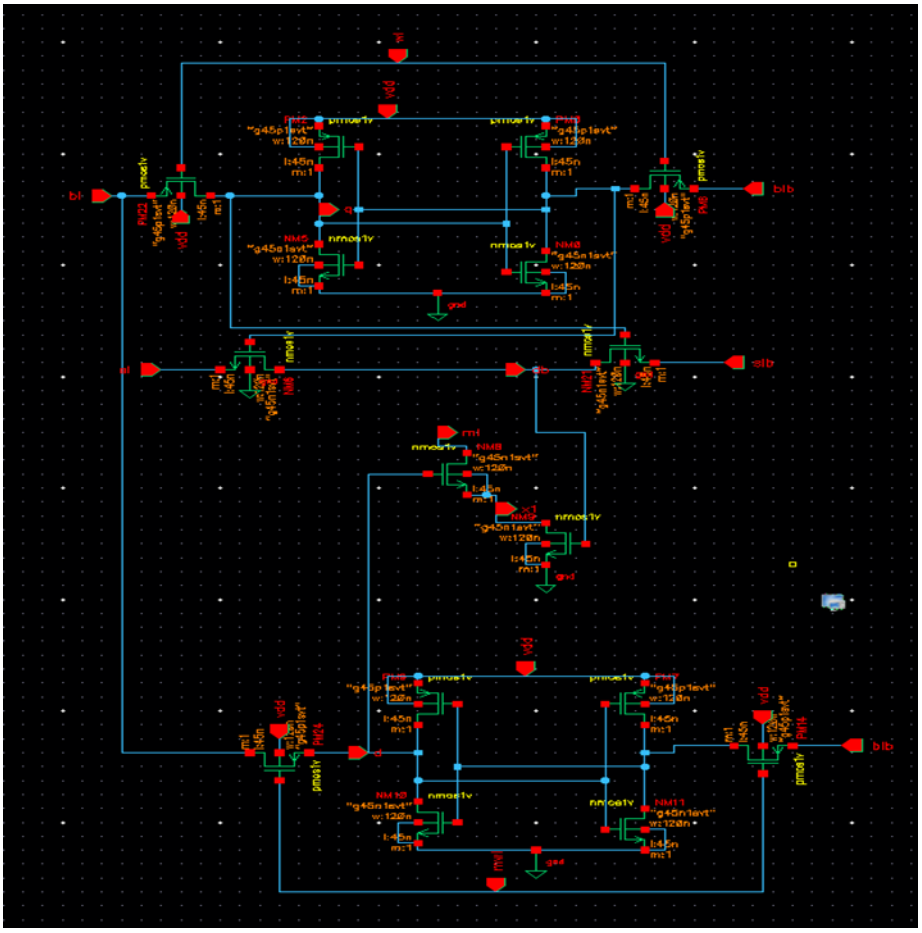

Figure 5: 1-bit TCAM based on architecture in paper [1].

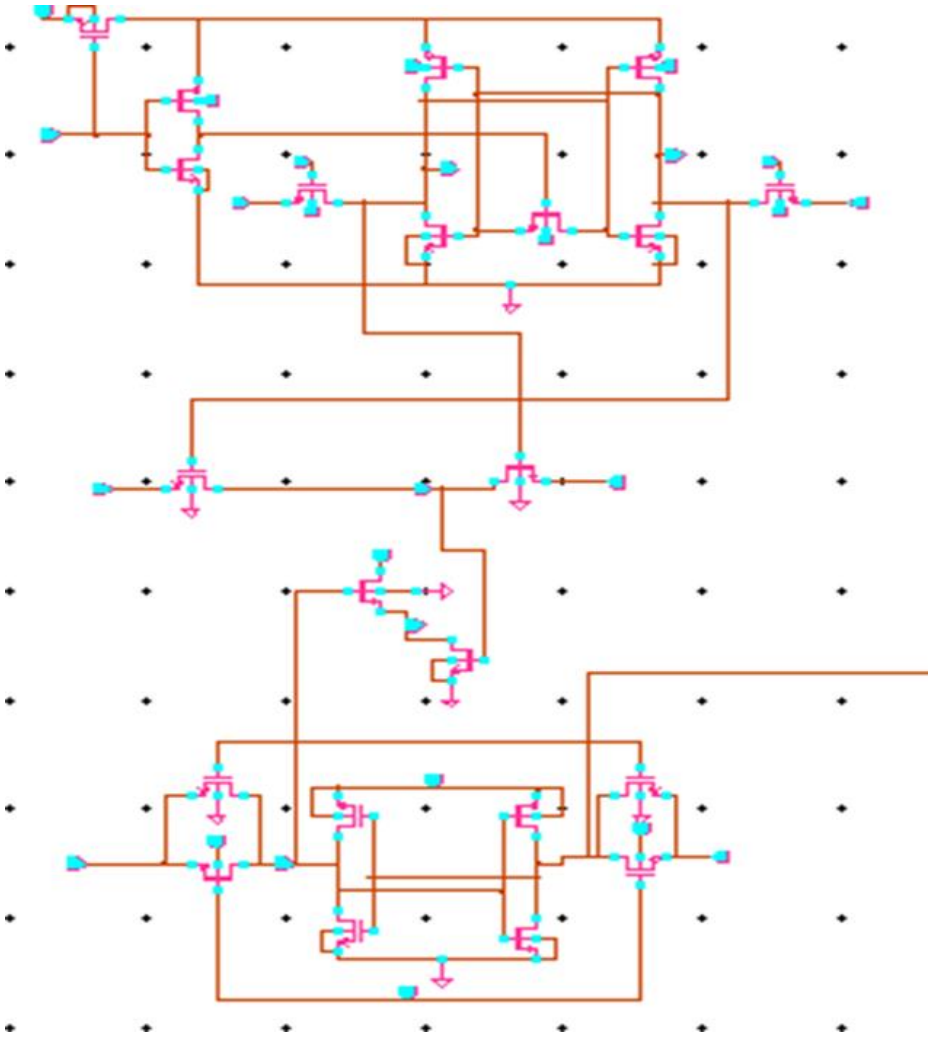

Figure 6: Proposed architecture of TCAM

4. Results and discussion:

In this brief, all TCAM designs are implemented with Cadence Virtuoso 45nm technology and simulated with 1.0Vpower supply. The figure 8 shows the output ml of 1-bit TCAM which goes high when bit line bl and search line slare a match, this comparison happens only when wl and mwl are low. This is due to the wl and mwl are connected to PMOS access transistors which get enabled with active low signal. When either one of wl or mwl is not low, masking of the data happens i.e 'x' term is considered and in this state the ml enters into the ternary state. This helps inreducing unwanted power consumption.

Design	Power	Delay
Proposed architecture in paper 1	92.91µW	56.7ps

Table 3: Results of 1 bit TCAM

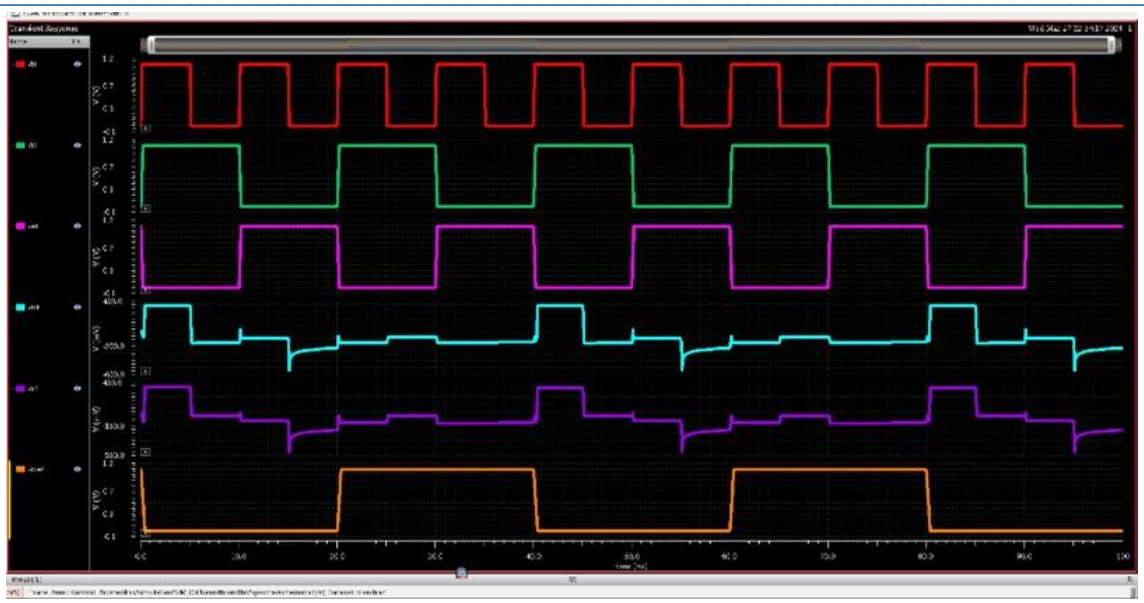

Figure 7: Results of 1 bit TCAM

Figure 9 illustrates the output waveform from implementing the architecture proposed in [1], aimed at reducing leakage power.The signal x1 shows the comparison output between sl3 and bl3, occurring only when both mwl and wl are low. Despite its power-saving benefits, this architecture introduces a noticeable delay, which is problematic since TCAMsrely on fast search times. This delay must be addressed, and the proposed architecture in this work aims to solve thisissue by optimizing the design to attain low power utilzation while ensuring rapid search performance.

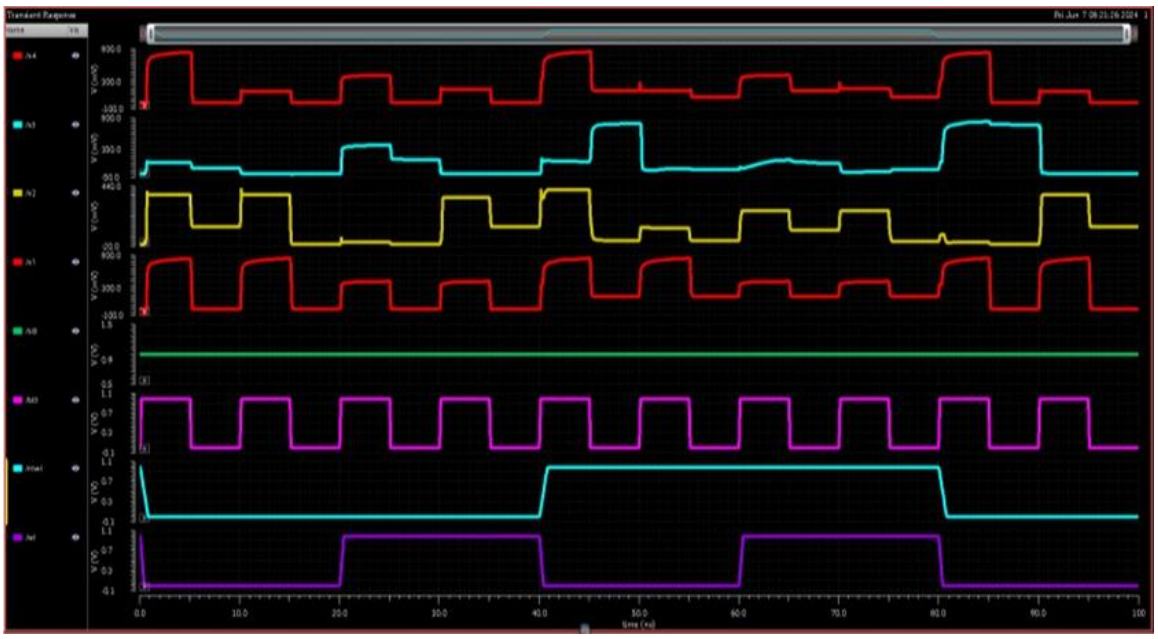

Figure 8: Results obtained for 4 bit TCAM proposed in paper [1].

The implemented TCAM architecture surpasses state-of-the-art designs by achieving reduced search time and significant power dissipation. Figure 10 displays the output waveform of the proposed 4-bit TCAM, which employstransmission gates and power gating techniques. These innovations result in negligible overall power consumption and substantially reduced delay, enhancing the TCAM's performance and efficiency.

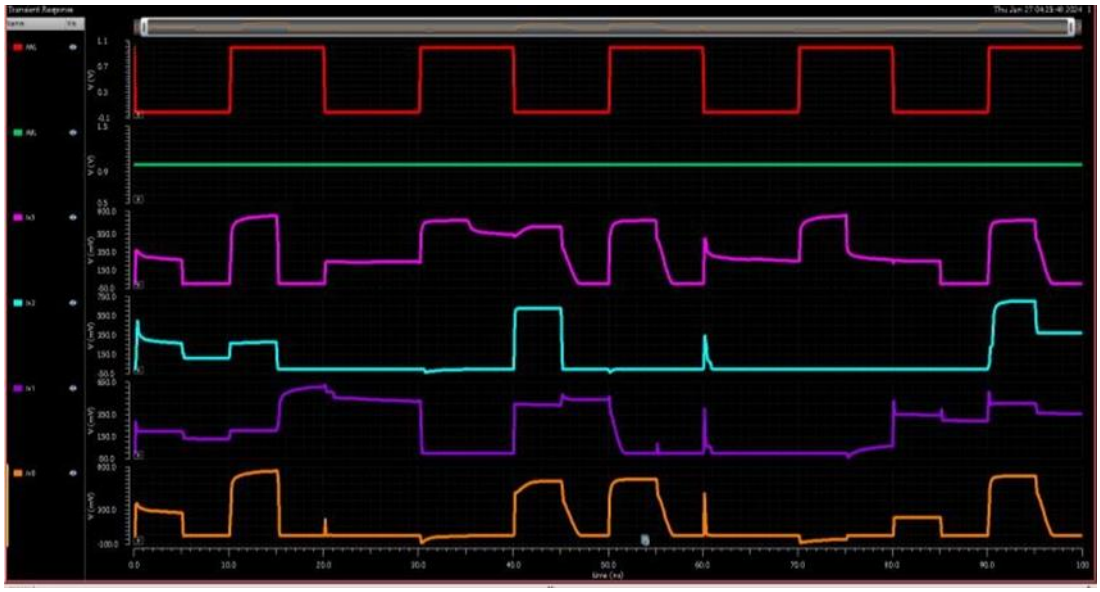

Figure 9: Obtained waveform for proposed architecture.

Table 3 shows comparison of the results of paper 1 architecture with that of the proposed architecture. It demonstrates a notable performance improvement, with a search speed approximately 84% faster than previous designs, despite a substantial 13% increase in power consumption.

Design	Power	Delay
Paper 1 architecture	82.42µW	375.1ps
Proposed architecture	92.91µW	56.7ps

Table 4: Comparison with the architecture proposed in paper [1]

5. Conclusion

In conclusion, this study presents a novel approach to designing an energy efficient TCAM structure for secure data transmission in wireless communications. The proposed TCAM architecture, integrating power gating and Transmission Gate Logic (TGL), demonstrates improved performance metrics compared to the existing extension. Through comprehensive simulations and analyses, the proposed TCAM accomplishes a equilibrium between power consumption, delay, area, achieving a search speed around 84% faster than earlier designs, with a considerable 13%raise in power consumption.

The comparison table highlights the superiority of the proposed TCAM over the previous work with respect to power consumption and delay. While the previous work exhibits lower power consumption, the proposed TCAM outperforms in terms of delay, indicating faster operation. Additionally, the proposed TCAM achieves a significant reduction in MOS count, indicating a more compact and resource-efficient design.

6. Future Scope

As mobile networks evolve, fast and efficient data routing need increases. TCAMs can support high-speed lookups and help manage the complex routing tables required by advanced mobile networks. TCAM can play a important role in SDN by enabling rapid policy enforcement and flexible network management. TCAM can be used in Intrusive Detection System and Firewalls for rapid pattern matching to detect malicious activities and filter traffic respectively, advancing the efficacy of network security devices in real-time.

TCAM's ability to perform rapid searches makes it suitable for edge computing devices that require low-latency

processing for real-time applications. Advances in low-power TCAM can be used to extend the battery life of IoT devices, making them more practical for remote and embedded applications. TCAM combined with AI ML can be used to support high-speed pattern matching, which is important for real-time data processing and decision-making. Also, TCAMs can support certain types of neural network architectures, potentially improving the speed and efficiency of inference processes.

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