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Implementation of Asic Based Duty Cycle Correction Circuit

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Abstract: Duty cycle is a component of VLSI circuits where performance plays an important role. This paper illustrates an accurate Duty cycle correction circuit with high performance measurement accuracy and correction of ranges. Experimental and theoretical results are shown which closely correlated.

Keywords: Implementation, Correction Circuit

I. Introduction

In this approach of study a circuit for fine duty-cycle control in high-frequency systems is presented. The suggested digital circuit is more reliable, simpler to use, and capable of higher-frequency resolution improvements. The project is dealing with the design and analysis of clock 35 signal Duty cycle measurement and Correction. For a digital circuit with a clock signal is concerned the most sensitive area is the clock. The complete operation of the block is synchronized with the clock. For better operation or for better data processing the stability of the clock is pretty much important. If for a block is considered the clock signal need to travel different places inside the block that will degrade the duty cycle of the clock. The clock signal can be further weakened by environmental and process variables, making it challenging to produce and disseminate high-frequency clocks with a fixed duty cycle [2].

The scope of study for duty cycle correction circuits includes design considerations, implementation techniques, and performance analysis. This involves understanding the impact

of process variations, signal amplitude, and frequency range on the performance of duty cycle correction circuits. Additionally, the study may involve comparing the accuracy, power consumption, and ease of integration of digital duty cycle correction circuits with traditional analog techniques[2].

II. Technology and Tools Used

a. -90 nm Technology

Leading semiconductor industries like TI, IBM, Intel, , TSM, Elpida, AMD, Samsung ltd and Toshiba Ltd have commercialized the 90 nm process for CMOS production

between 2003 and 2005 with historic associated with a 70% upward trend every 2 to 3 years. ITRS specifies the designation. For base layer lithography, mostly at the 90nm node, many companies have adopted the 193nm wavelength. The significant costs associated with this change were reflected in performance concerns.

b. OBJECTIVES

- To identify and analyze the duty cycle correction circuit used in digital circuits.
- To understand the working principle of the duty cycle correction circuit and its components.
- To investigate the performance characteristics of different duty cycle correction circuits and compare their effectiveness in correcting duty-cycle errors.
- To evaluate the impact of duty-cycle errors on digital circuit performance
- To propose recommendations for improving the design and implementation of duty cycle correction circuits in digital systems.

III. Duty Cycle Corrector

The duty cycle adjuster circuit is a key component of the duty-cycle correction circuit and is responsible for adjusting the duty-cycle of the input clock by controlling the delay between two complementary signals. The adjuster circuit receives 29 a DC voltage from the loop filter, which is generated by the charge pump based on the error signal from the phase detector. The adjuster circuit then adjusts the delay between two complementary signals to correct any duty-cycle errors in the input clock.

In other words, when there is a duty-cycle error in an input clock signal, the phase detector generates an error signal that is used to generate a DC voltage through a charge pump. This

DC voltage is then fed into a loop filter, which generates a stable voltage that is used to control the delay between two complementary signals in the adjuster circuit[4].

By adjusting this delay, any duty-cycle errors in the input clock can be corrected. The amount of correction required can be controlled by selection bits from 0 to 15, with each bit's selection correcting the input clock signal by a fixed amount. This process ensures that digital circuits operate with optimal performance and reliability by correcting any duty-cycle errors in high-frequency clocks with very fine resolution.

In older reference line-based duty cycle control circuits, duty cycle variation is accomplished employing both rising and falling generators or falling-edge generators.

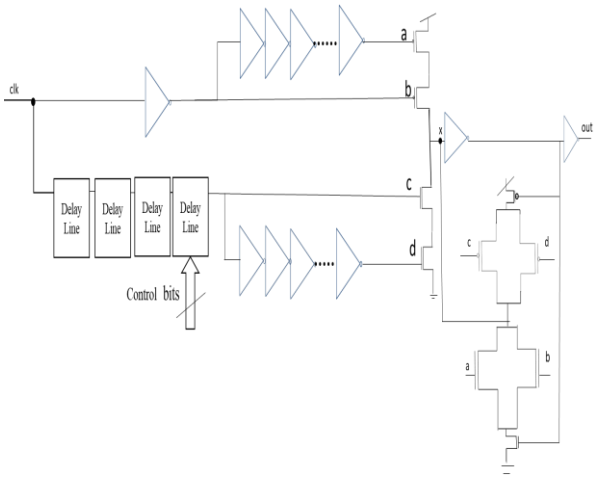


Figure1. Circuit diagram of duty cycle adjuster

Figure1 gives a schematic of the duty cycle regulator. The duty cycle adjuster circuit is a key component of the duty-cycle correction circuit and is responsible for adjusting the duty-cycle of the input clock by controlling the

delay between two complementary signals. The adjuster circuit receives 29 a DC voltage from the loop filter, which is generated by the charge pump based on the error signal from the phase detector. The adjuster circuit then adjusts the delay between two complementary signals to correct any duty-cycle errors in the input clock. In other words, when there is a duty-cycle error in an input clock signal, the phase detector

generates an error signal that is used to generate a DC voltage through a charge pump. This DC voltage is then fed into a loop filter, which generates a stable voltage that is used to control the delay between two complementary signals in the adjuster circuit..

If used in these circuits, the period of the lowest operating frequency is the minimum length of the delay line required to give the entire 50% correction range..

A.CORRELATION BETWEEN ADJUSTER and CORRECTION CIRCUIT.

1. The duty-cycle correction circuit is responsible for correcting any duty-cycle errors in the input clock signal.

2. The adjuster circuit is a key component of the duty-cycle correction circuit.
3. The adjuster circuit receives a DC voltage from the loop filter, which is generated by the
4. The adjuster circuit then adjusts the delay between two complementary signals 39 to correct any duty-cycle errors in the input clock.
5. In other words, the adjuster circuit controls the delay between two complementary signals to adjust the duty-cycle of the input clock.
6. By adjusting this delay, any duty-cycle errors in the input clock can be corrected.

Therefore, there is a direct correlation between the adjusted circuit and correction circuit in that they work together to correct any duty-cycle errors in the input clock signal.

In accordance with the DCC control signal Sign, the main disadvantage of this controller edges is that a custom phase detector must be created because of the DLL that only analyzes the rising edges and falling edges, resulting in a complex DLL design Abbreviations and Acronyms.

VLSI -very large-scale integration

ASIC- Application Specific Integrated Circuit(ASIC).

MUX-multiplexer

DCC-duty cycle corrector

DLL-delay locked loop

ITRS–InternationalTechnology,RoadMap for Semiconductors.

nm- Nano meter

LVS- Layout versus schematic

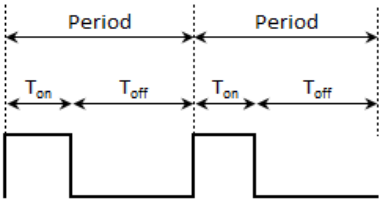
PCB- Printed Circuit Board.

IC- Integrated circuit

BOM- Bill of Materials.

B.Duty cycle.

The idea of duty cycle correction circuits, its significance in ASIC design, and typical implementation methods. ASIC Implementation of Duty Cycle Correction Circuit and Frequency Range Design Considerations for Duty Cycle Correction Circuit Performance Jitter. To identify the proper circuit clock skew on the signal topology, the frequency range of the signal that the circuit should be designed to better needs to be corrected, taken into account, and reduced. A signal's duty cycle tells you how much of the time it is ON.



Period = 1 / Frequency
Period = $T_{on} + T_{off}$
Duty Cycle = $T_{on} / (T_{on} + T_{off}) * 100$
(On Percentage)

Figure 2: Duty cycle

The duty cycle ratio regulator is an important part of the circuit, which does the job on the principle that pull-up and pull-down power of the inverter is regulated by the feedback digital signals. This circuit applies two stages of rectification , the stage one performing coarse rectification and the another stage performing fine rectification.

on time / (on time + off time) = Duty Cycle

C.Analysis Of Timing Paths

Based on start point and endpoint, timing analysis can be executed by dividing the design into distinct paths. A clock, a sequential cell, a primary input port, a data pinof a level sensitive latch ,a clock input pin of a sequential cell or a pin that specifies the input delay are included in the start point and end point consists of a clock , a sequential cell, a pin

that specifies the output delay, a primary output port or a data input pin of a sequential cell.

Different Types of Paths for Timing analysis:

- Data path clock path
- Clock Gating
- Path Asynchronous Path

D. Types of delays

Calculation of max and min delay in a circuit by the tool is same as the way we discussed earlier. Many types of delay are there listed below

• Input Delay

• Net Delay

• Intrinsic Delay

• Connect Delay

• Cell Delay

• Slope Delay

• Wire Delay

• Interconnect Delay

Out of these long lists of delays, some are interconnecting to each other and just synonym of other. That means wire delay is nothing but net delay and interconnects delay. So, we generally split into net delay and cell delay. Stage delay is the combination of cell delay and net delay .

We have taken 10ns as period and 1.5ns as pulse width which makes 15% duty cycle to the clock signal and fed it to circuit.

1. As we simulate the results by selecting the input and output lines on ADE L suite, we obtain the

2. It means that we get 5.5ns as ON time and 4.5ns as OFF time.

3. The formula to calculate duty cycle in percentage is

Duty Cycle={ton / ton+toff}100

IV. Results

By adjustment of the parameters of the delay line, we can calculate the output's duty cycle. While feeding the same 8GHz clock to the controller.

The graph demonstrates that the input clock's duty cycle may be changed. from 15% - 56% in steps of less than 1%.

The feedback loop chooses the best controller settings. Our observations gives that loop can be accurately to 50% of the duty cycle for multiple input duty cycles.

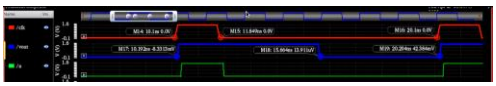
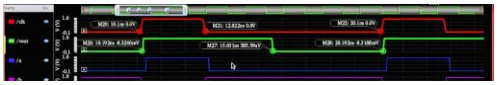
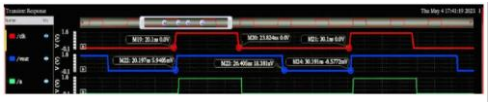
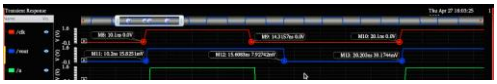
ENHANCED DUTY CYCLE	SIMULATED OUTPUTS
15-54%	
25-54%	
35-63%	
42-56%	

Figure 3: Enhanced duty cycle simulated outputs.

MAXIMUM DUTY CYCLE OBSERVED	CONFIGURATION	DUTY CYCLE ENHANCED
15-62%	0000	47%
35-63%	0000	28%
45-61%	0000	16%
50-62%	0000	12%
15-54%	0100	39%
25-54%	0100	29%
35-56%	0100	21%
42-56%	0100	14%

Figure 4: Table of duty cycle of various lines .

Ⅴ. Applications

Some of the application in real time of vlsi and microelectronics plays important role for duty cycle correction circuit some ranges of application are Digital signal processing: It is used in digital signal processing applications to improve the accuracy and efficiency of operations such as filtering, modulation, and demodulation.

i.Microprocessors and microcontrollers: In microprocessors and microcontrollers, accurate timing is essential for executing instructions and controlling peripherals.

ii.Test and measurement equipment:It is used in test and measurement equipment to generate and measure signals with high precision by ensuring accurate timing.

Overall, the duty-cycle correction circuit has a wide range of applications in real-time systems where saccurate timing is critical.

Ⅵ. Advantages and limitations

A. Advantages:

i. Digital implementation: The duty-cycle correction circuit is digital and does not require external references or matching devices. This makes it more robust and less sensitive to environmental and process variations..

ii. Wide input range: The duty-cycle correction circuit can correct the duty-cycle of an input clock with a wide range of duty-cycles, typically from 25% to 75%. This makes it suitable for a wide range of applications

iii Noise sensitivity: the duty-cycle correcting circuit is perfect for a wide range of applications because it can correct the input clocks duty cycle with a wide spread of active period generally from 25 to 75.

B. Limitations

i. Limited input frequency range: The duty-cycle correction circuit is designed to correct the duty-cycle of high-frequency clocks, typically up to 8 GHz. It may not be suitable for correcting the duty-cycle of clocks with frequencies outside this range..

ii. Complexity: The duty-cycle correction circuit may be more complex than traditional analog techniques for duty-cycle correction, which can make it more difficult to design and implement.

Ⅶ.Conclusion

The Duty cycle measurement and correction circuit is designed and 40 tested. The Design has given good results. This study has explored the concept of duty cycle correction circuits and their importance in ASIC design. We have discussed the d9e6sign considerations for duty cycle correction circuits, including frequency range, jitter performance, sensitivity to process variations, and signal amplitude. We have also examined common techniques used for implementing duty cycle correction circuits and compared their accuracy, power consumption, and ease of integration with traditional analog techniques..

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