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FPGA implementation of KNN Algorithm-Based Prediction for DPWM Methods

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Abstract:

This paper presents the prediction of the DPWM methods using the FPGA device. For the sake of prediction, the parameters such as Clocking frequency, switching frequency, positive duty cycle value, and negative duty cycle value are considered by taking 23 samples of the real-time results obtained for the DPWM techniques. Based on the dataset, the parametric values are fed into the KKN algorithm to predict the suitable DPWM technique by identifying the K-nearest neighbor. The proposed KNN algorithm for the DPWM technique prediction is developed using the VHDL code and synthesized in the FPGA board for real-time validation. Also, the ASIC IC layout design for the proposed method is generated using the Cadence EDA tool. The performance analysis for the power, area, and delay are evaluated using the Xilinx and Cadence Tool.

Keywords: *Digital Pulse Width Modulation, Prediction Algorithm, KNN Machine Learning Algorithm, Field Programmable Gate Array*

I Introduction

The inclusion of artificial intelligence has given enormous advantages in classification, regression, identification, and prediction by utilizing the datasets. The AI algorithms are divided into Machine learning and Deep Learning algorithms with their purpose efficiently used according to the target application. Though AI algorithms are used effectively in Real-time scenarios, the impact of their use is minimal in renewable power applications. This is because the dataset required to be generated based on the several attributes of the power applications.

Recently, the adaptation of AI algorithms in power applications has become proficient in analyzing the faults and failures occurrence and thus used to avoid increases in the maintenance cost of power devices. There are several ways that machine learning and deep learning algorithms be used with power circuits and systems. The choice of the AI algorithm chosen also depends on the ultimate objective of the real application used. The residential electricity bill is evaluated using the 23-nodes cloud computing cluster combined with the KNN to give accurate prediction of the future load [1]. The failures in the transmission line are categorized as one among the five issues namely Secure, Critically Secure, Insecure Highly Insecure, and Most Insecure using the KNN algorithm [2]. The combined algorithm of KNN and LSTM uses the spatiotemporal features of traffic flow data to correlate between the nodes of the destination road section and has more accuracy in predicting than the other models [3].

The PV power generation can be accurately predicted using the fusion of Support Vector Machines and K-nearest neighbors algorithms [4]. The power load of the Electricity market in Australia is utilized to evaluate the mean value per 8 hours to regulate the electricity using the KNN algorithm [5]. The 6 PV panels are distinctly predicted for power generation using the machine learning algorithms namely the ensemble-based random forest

technique [6]. The Maximum Power point for the solar modules is tracked using the machine learning algorithm by taking into account the dataset consisting of attributes like Solar voltage, Solar Current, temperature, irradiance, and PI values [7].

The KNN algorithm is utilized to investigate the vibrations in the wind turbines to eradicate the failures and faults [8]. The rotor bearings in the wind turbines are checked for faults using the KNN algorithm to increase energy production and decrease the maintenance cost [9]. The KNN algorithm is used to detect the output current of the inverter without a sensor by varying the Modulation rate, carrier frequency, and signal frequency of the Power Inverter [10].

In this work, the six DPWM techniques are predicted using the KNN algorithm. For this purpose, the real-time results for the six DPWM techniques are listed in the dataset with the parameters of FCLK, FSW, DUTY+, and DUTY-. The predicted output from the KNN algorithm is implemented using the FPGA code. The VHDL code is developed and synthesized using the Artix 7 FPGA board for validation.

II The proposed KNN-based Predication for DPWM methods

The proposed method predicts the choice of DPWM algorithm to be used based on the attributes of Clocking Frequency, Switching Frequency, Positive Duty cycle, and negative duty cycle without feedback. The dataset is considered by taking into account the real-time experimental output for DC-DC buck converter control using the DPWM techniques. The DPWM techniques considered for the prediction are counter-based DPWM, Delay line-based DPWM, hybrid-based DPWM, Modified CDPWM, Modified Delay line-based DPWM, and Modified Hybrid-based DPWM. The modified DPWM methods are derived from the basic DPWM techniques to reduce the Switch ON and Switch OFF delay of the Pulse Width Signal. In simple words, the modified DPWM generation produces the pulse width modulation signal with low delay at the rising edge and falling edge. If the delay is present at the rising edge, it is named a Switch ON delay and if the delay is present at the falling edge, it is named a Switch OFF delay. The following section gives a detailed explanation of the Modified DPWM techniques.

A) Modified Counter based DPWM generator

The block diagram for the Modified Counter DPWM is given in Figure 1. This Modified Counter DPWN is used for the reduction in the delay of the falling edge and thus used for Switch OFF delay. There are two counters in the given design, with the descending counter having the primary counter that produces duty value similarity as SET and zero value similarity as RESET1 (R1) for the SR flip flop. Concurrently, as the SET values becomes “1”, the secondary Ascending Counter is induced to produce the similarity of this counting with the duty value in RESET2 (R2). Now these two R1 and R2 are fused with the AND logic to generate the RESET signal for the SR Flip Flop.

This arrangement ensures that the Modified Counter DPWM consider all the matching similarity of the RESET (including R1 and R2) to reduce the Switch OFF delay in the DPWM. Similarly, by changing the direction of the Primary counter as the Ascending counter and the Secondary counter as the Descending counter, the modified Counter DPWM can be used for the reduction of the Switch ON delay.

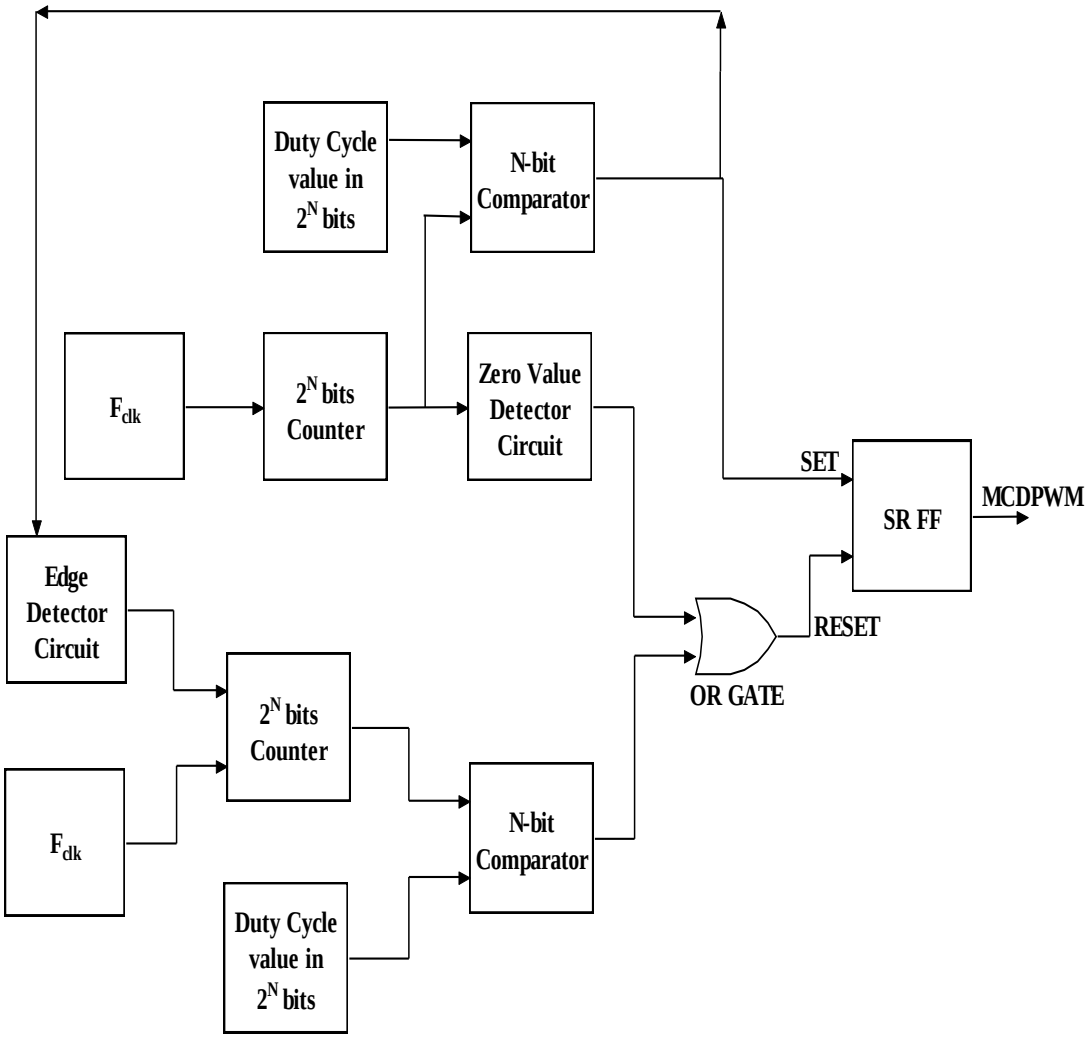

Figure 1 Modified Counter-based DPWM generator for Turn-OFF delay reduction

B) Modified Delayline-based DPWM generator

The block diagram for the Modified Delayline DPWM is shown in Figure 2 which lowers the Delay in the rising edge namely the Switch ON delay. The different happening of the SET values is taken for the Modified Delay line DPWM. The Switch ON is the uniqueness in the Modified Delay line DPWM concerning conventional DPWM that holds for 1 cycle to consider the differences in SET values. Practically, the logic device count is constant for inducing the inputs. The duty value is utilized for the below data selector and the 1-duty value is utilized for the above data selector. There are two ways of lowering the delay in the Modified Delay line DPWM namely Switch ON delay-based MDDPWM and Switch OFF delay-based MDDPWM.

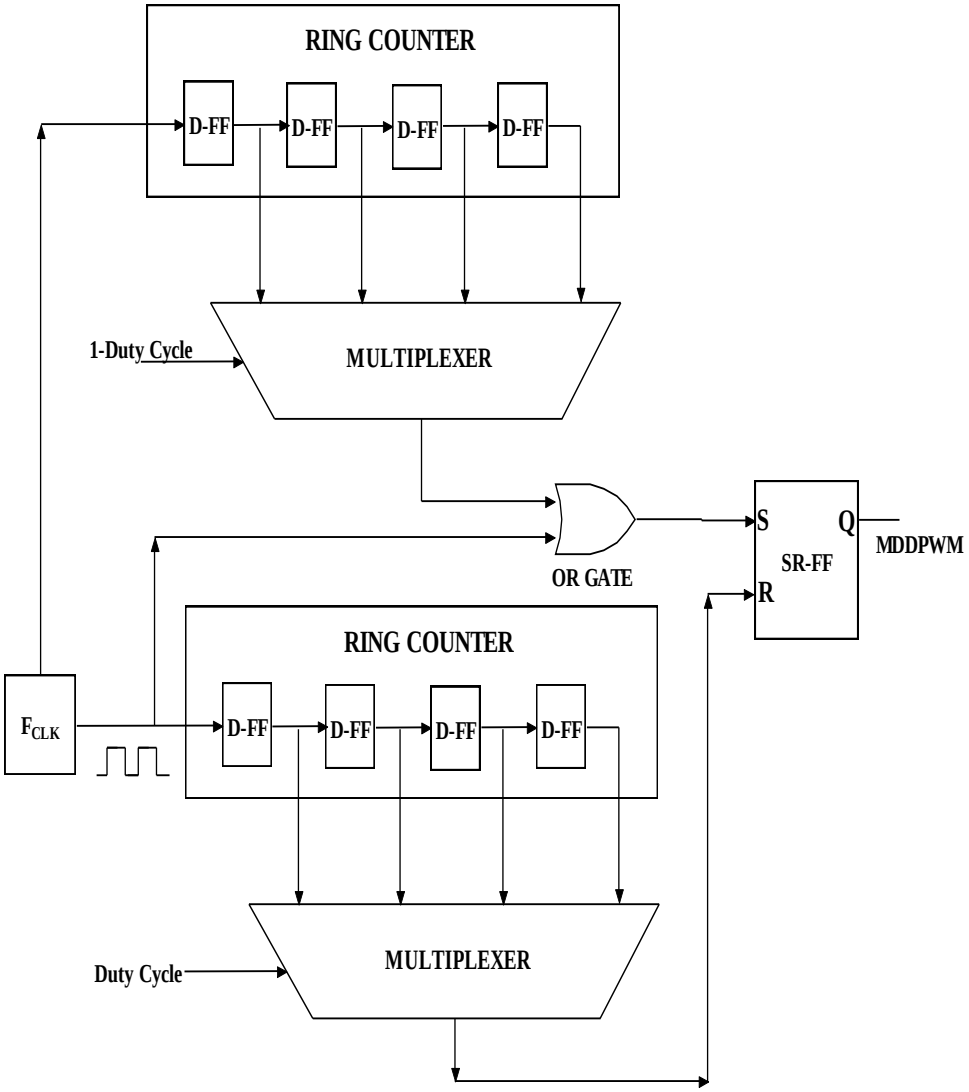

Figure 2 Modified Delayline-based DPWM generator for Turn-ON delay reduction

C) Modified Hybrid Digital Pulse Width Modulation

The fusion of the Switch ON-based Modified Counter DPWM and Switch OFF-based Modified Delayline DPWM gives the Modified Hybrid DPWM. This Modified Hybrid DPWM is presented with the lowering of Switch ON and Switch OFF. The utilization of the OR logic in SET and RESET values is given for the SR-Flip Flop. Figure 3 presents the link between the Modified Counter DPWM and Modified Delay line DPWM by utilizing OR logic. By interlinking Figure 1 and Figure 2, the modified hybrid DPWM authenticates the merits in the enhancement of the switching of the DPWM signals.

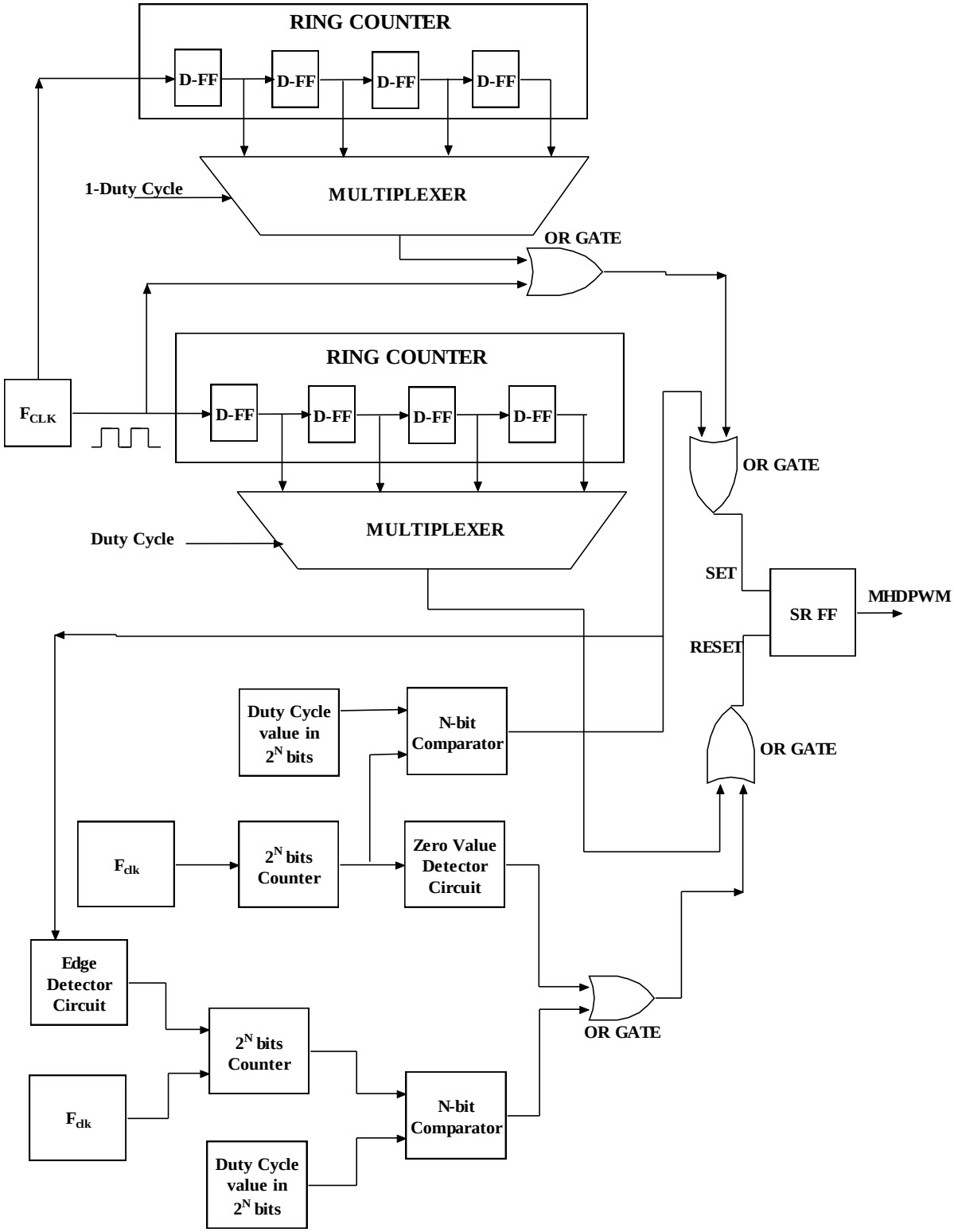

Figure 3 Modified Hybrid-based DPWM generator for Turn-ON &Turn-OFF delay reduction

The proposed method considers the output responses of all the DPWM techniques with different clocking frequencies and switching frequencies. The parameters namely FCLK, FSW, DUTY+, and DUTY- are considered for the proposed method. The four parameters are evaluated for the near values using the KNN

algorithm as given in Figure 4. The comparison is performed at the initial stage for all the four parameters. The proposed KNN is used to evaluate the distance for all the data set values to find the Nearest neighbor. The manipulated values of the distances are sorted according to the ascending order to find the top three values near the given parametric values. The n-value for the presented work is 3. Based on the majority of the 3 outcomes of the KNN algorithm, the prediction is given for the use of the DPWM technique for the given parametric values.

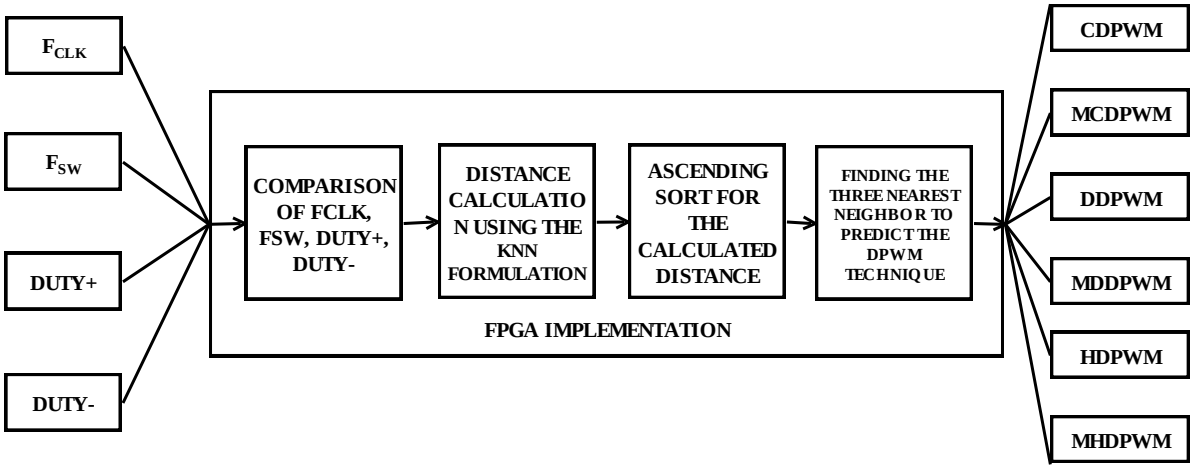

Figure 4 Block diagram for the proposed DPWM technique prediction using the KNN algorithm

III Results and Discussion

The proposed method predicts the method for the DPWM techniques based on the dataset as shown in Table 1. Table 1 depicts the values for the parameters of FCLK, FSW, DUTY+, and DUTY- for all the DOWM techniques namely CDPWM, DDPWM, HDPWM, MCDPWM, MDDPWM, and MHDPWM. The values for the FCLK are derived from the 3A DSP FPGA board that could generate in real-time such as 48MHz, 66MHz, 80MHz, and 100MHz. The FSW, DUTY+, and DUTY- values depend on the DPWM technique used. There are 23 samples in the dataset for the proposed method to predict the algorithm using the FPGA device. The VHDL code is used to develop the proposed algorithm in mixed modeling. The simulation output for the proposed method is shown in Figure 6. The simulated VHDL code for the proposed method is synthesized using the Xilinx Vivado Tool to generate the RTL schematic as given in Figure 7. The power report of the proposed method is presented in Figure 8 with the dynamic power consuming 99% and static power consuming 1%. Table 2 shows the device utilization chart for the proposed method using the Xilinx Vivado tool. The Xilinx Vivado verified VHDL code is considered by the Cadence tool to generate the schematic block suitable for the IDC layout using the Genus tool as given in Figure 8. The Innovus tool of the cadence is used to generate the layout for the proposed method as given in Figure 9.

Table 1 Dataset for the DPWM techniques prediction using the parameters of F_{CLK}, F_{SW}, DUTY+ & DUTY-

S.No	F_{clk} MHz	F_{SW} KHz	Without Feedback		Method
			Duty +	Duty -	
1	48	2.55	41.8%	58.2%	CDPWM
2	48	2.55	43.8%	56.2%	MCDPWM
3	66	3.47	41.7%	58.3%	CDPWM
4	66	3.47	45.7%	54.3%	MCDPWM
5	80	4.31	43.4%	56.6%	CDPWM

6	80	4.31	41.4%	58.6%	MCDPWM
7	100	5.21	29.2%	70.8%	CDPWM
8	100	5.21	42.7%	57.3%	MCDPWM
9	48	2.55	42.9%	57.1%	DDPWM
10	48	2.55	83.5%	17.5%	MDDPWM
11	66	3.52	42.2%	59.2%	DDPWM
12	66	3.52	84.5%	16.9%	MDDPWM
13	80	4.31	82.8%	17.2%	MDDPWM
14	100	5.32	29.2%	70.8%	DDPWM
15	100	5.32	54.2%	41.7%	MDDPWM
16	48	2.55	42.3%	57.7%	HDPWM
17	48	80.6	50.7%	49.3%	MHDPWM
18	66	3.52	42.3%	57.7%	HDPWM
19	66	111	50.5%	49.5%	MHDPWM
20	80	4.24	42.4%	57.6%	HDPWM
21	80	135	50%	50%	MHDPWM
22	100	5.32	41.7%	58.3%	HDPWM
23	100	172	51.7%	48.3%	MHDPWM

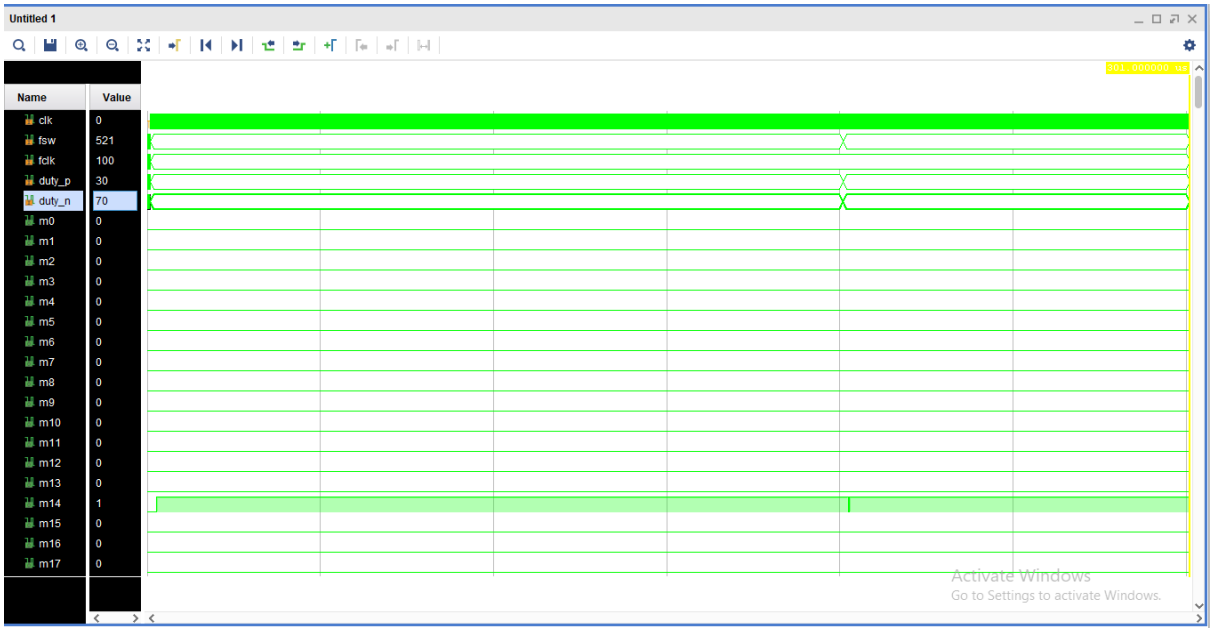

Figure 5. Simulation output for the proposed KNN-based DPWM Prediction methods

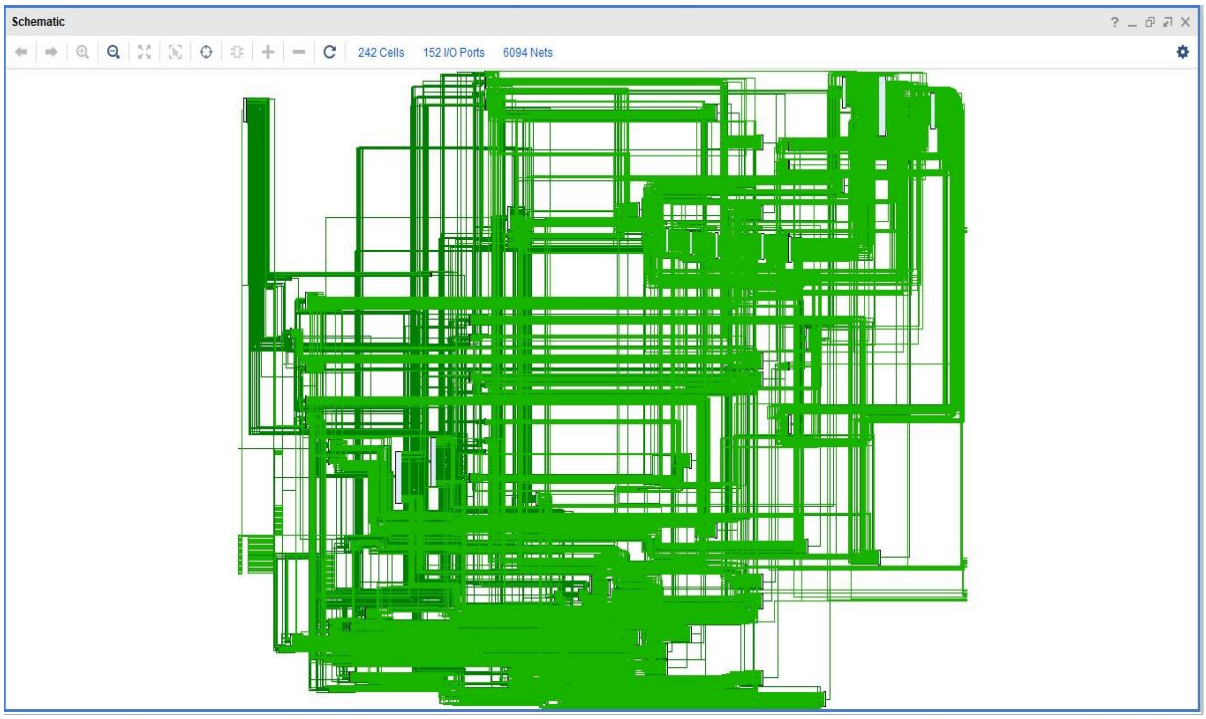

Figure 6 RTL Schematic output for the proposed KNN-based DPWM Prediction methods using Xilinx Vivado Tool

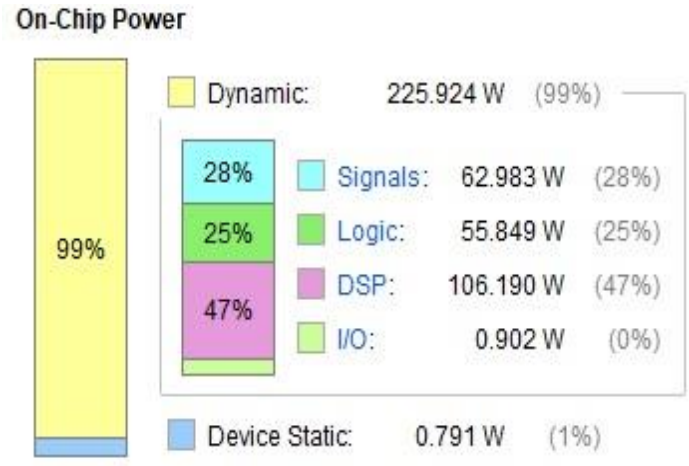

Figure 7 Power Report for the proposed KNN-based DPWM Prediction methods using Xilinx Vivado Tool

Table 2 Device Utilization Chart for the proposed KNN-based DPWM Prediction methods using Xilinx Vivado Tool

Resource	Utilization	Available	Utilization %
LUT	8592	63400	13.55
FF	2268	126800	1.79
DSP	144	240	60.00
IO	152	210	72.38
BUFG	1	32	3.13

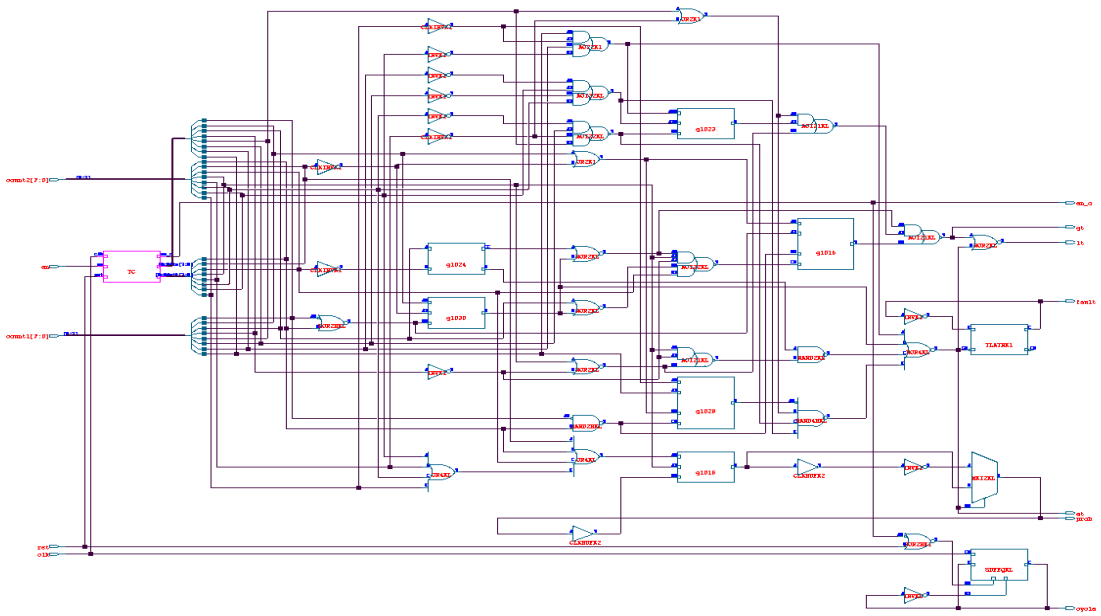

Figure 8 RTL Schematic output for the proposed KNN-based DPWM Prediction methods using Genus Cadence Tool

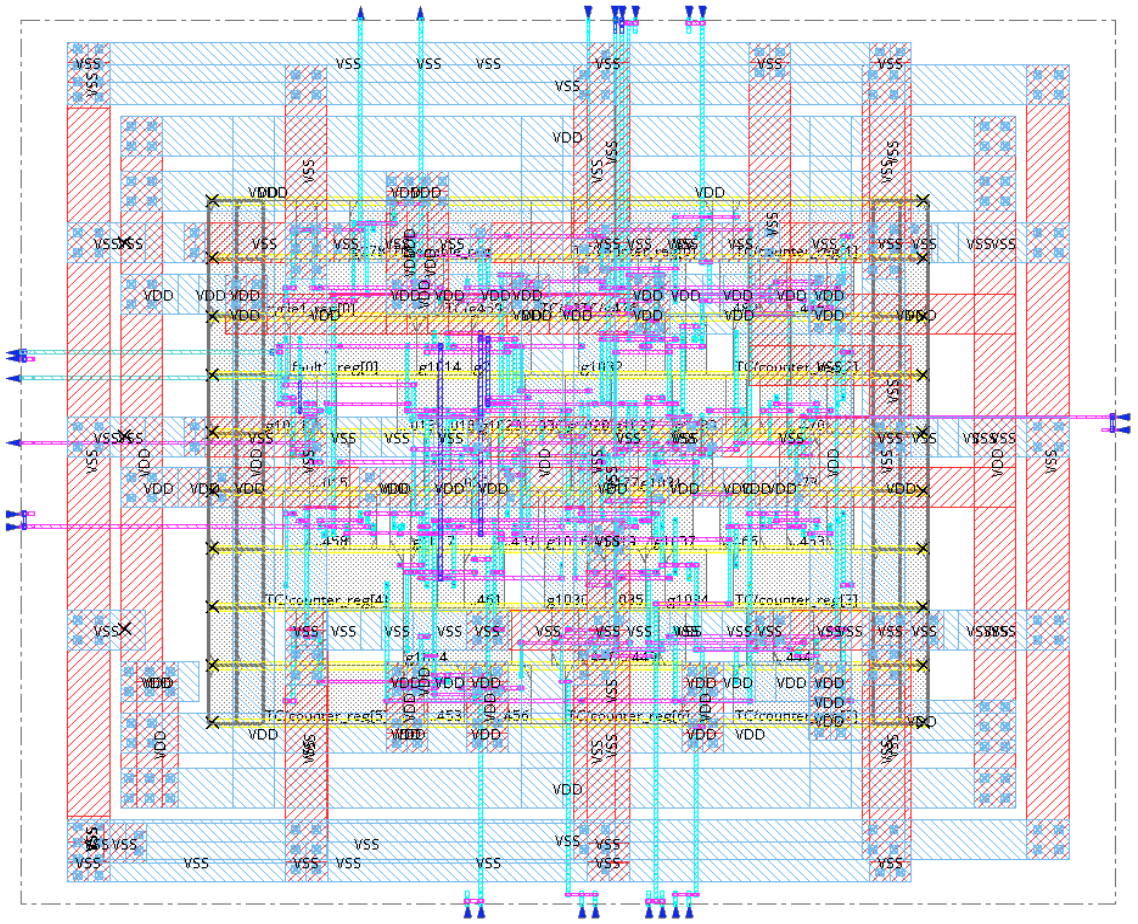

Figure 9 IC layout for the proposed KNN-based DPWM Prediction methods using Innovus Cadence Tool

IV Conclusion

The proposed KNN algorithm-based DPWM techniques prediction is successfully simulated and verified using the Xilinx Vivado Tool. The real-time validation for the proposed method is attained using the Artix 7 FPGA board. The synthesis of the proposed method is feasible in the Cadence Tool environment with the help of the Genus tool. The IC layout for the proposed KNN prediction of the DPWM is derived with ease and could be used to fabricate for the purpose and objective of this work.

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