Tuijin Jishu/Journal of Propulsion Technology
ISSN: 1001-4055
Vol. 44 No. 3 (2023)

A Study & Analysis on low Power processor Design Using Various Techinques

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Abstract:-In the area of microprocessor design, the application of low power techniques has bring togethermomentouscontemplation for its potential to enhance performance and efficiency. With rapid advancements in digital circuit applications, low Power is one of the prominent aspects in the design of digital processors. Designing a low-power digital processor is essential for various applications, such as mobile devices, IoT devices, and battery-powered systems. Lower power consumption affects the battery utilization with minimization in heat generation and environmental impact. In this paper the scope and significance of low power microprocessor research is discussed. The contribution of how each component of the design affects to overall power consumption, various techniques for reducing the dynamic and static power is presented.This paper aims to provide an insightful literature survey on microprocessor constitutionby employing low-power techniques, analyzing existing research and advancements in the field.Indisputably, the literature review plays a pivotal role in understanding the current state of knowledge pertaining to microprocessor design and low power techniques. By examining a amplecollection of scholarly articles, conference papers, and technical reports, this section aims to present a comprehensive overview of the research landscape.The focus will be primarily on investigating various methodologies employed for dropping power dissipation in microprocessors. This includes but is not limited to dynamic voltage scaling, clock gating techniques, leakage current reduction strategies, and architectural optimizations.

Keywords*: Low Power, Digital Processor,IoT, Power consumption, Dynamic Staic*

1. Introduction

Microprocessor design is a critical area that plays a vital role in modern computing systems. As technological advancements continue to drive the need for smaller and more efficient devices, reducing power consumption has become a primary concern. Low power techniques and strategies have emerged as effective solutions to address this challenge. Today's electronics industry focuses on low power. The requirementof low-power has caused a shift in the way power is used. The article describes the many issues facing designers at architectural, logical, and physical levels of design abstraction and introduces comprehensivelystudy of CAD methodologies

and stratergies for creating low-power CMOS based circuits &systems. It reviews some of the techniques and tools that have been proposed to overcome these difficulties and outlines the future challenges that must be met to design low-power, high performance systems. In the past, the main metrics of anydesign engineer were wrt area, performance, cost, and reliability,with nominal focus on power. In recent years, however, this has begun to change, and more power is being given a influence comparable to the area and performance. Many factors contributed to this trend. Perhaps the main driving factor has been the rapid growth of the class of personal computing devices, wireless communications systems, AI device's, IoT enabled devices, which require agile calculations & heterogenous functionalities with low power consumption. In these applications, the normal power dissipation is a vital design concern. The motivation for reducing power consumption differs from purpose to purpose.In the class of micro-powered battery-operated mobile applications, such as cellular phones and personal digital assistants, IoT devices.Overall, CMOS technology is the dominant choice for digital IC design due to its excellent balance of low power consumption, high noise immunity, and versatility, accomplishing it apt for a amplescope of electronic devices and applications. CMOS, which stands for Complementary Metal-Oxide-Semiconductor, is a fundamental technology employed in IC design. It is a kind of semiconductor technology that utilizes both p-type and n-type metal-oxide-semiconductor field-effect transistors to create digital and analog circuits. NMOS transistors are turned on by applying a +ve voltage supply to the gate relative to the source. PMOS transistors are turned on by applying a -ve voltage supply to the gate relative to the source. CMOS circuits operate in a complementary manner, which means that when one type of transistor is on, the other is off. This complementary behavior leads to extremelylittle static power utilization because there is no direct current path from the supply voltage to ground when a CMOS gate is idle. CMOS circuits can operate over a broadvariety of input voltages, making them versatile for various applications. CMOS technology allows for high integration density, meaning that many transistors and logic gates can be packed into a small chip area. This is essential for creating complex digital ICs with numerous functionalities. CMOS technology has the potential for high-speed operation, and advancements in CMOS manufacturing processes have continuously improved the speed of CMOS circuits. CMOS fabrication processes are well-established and relatively straightforward, which contributes to lower manufacturing costs.

2. Objectives

Various techniques and strategies are employed to trim down power utilization in CMOS circuits. The following are some commonly used low-power techniques

1. Supply Voltage Scaling: Sinking the power supply or voltage scaling or voltage reduction can significantly lower power consumption. However, this may also impact performance, so it's important to find the way between power reduction and speed.

2. Clock Gating: Clock gating involves selectively immobilizing the clock signal to specific circuit blocks or registers when they are not in use. This prevents unnecessary switching activity and reduces dynamic power consumption.

3. Power Gating: Power gating, also known as power shutdown or power gating, involves completely turning off power to unemployeddesignunits or functional units while they are not required. This can be achieved using transmission gates or dedicated power switches.

4. Multi-Voltage Domains: Divide the IC into various voltage domains with different supply voltages to match the power requirements of specific blocks. This allows you to reduce power in less critical areas while maintaining higher performance in others.

5. Sub-threshold Operation: Operating transistors in the sub-threshold region (below the threshold voltage) can reduce both static-power & dynamic-power dissipation. However, this comes at the cost of reduced speed and increased sensitivity to process variations.

6. Reduced Swing Logic: Using logic gates that operate with reduced voltage swings can reduce dynamic power consumption. These circuits use smaller voltage differentials between logic levels, which results in lower power dissipation.

7. Dynamic Voltage and Frequency Scaling (DVFS): Adjusting the voltage and clock frequency dynamically based on the workload or performance requirements can help balance power and performance. Higher voltage and frequency settings are used when needed, and lower settings are used during idle or light-load conditions.

8. Data Encoding and Compression: Using data encoding techniques and compression algorithms can reduce data transitions and bus activity, leading to lower dynamic power consumption.

9. Low-Power Logic Families: Some CMOS logic families are specifically designed for low-power applications, such as LVCMOS (Low-Voltage CMOS) and LVTTL (Low-Voltage TTL).

10. Pipeline Stages and Register Insertion: Adding pipeline stages and registers can reduce the clock frequency and voltage required for a given performance level, thereby reducing power consumption.

11. Low-Power Libraries: Utilize low-power standard cell libraries and design methodologies that prioritize power efficiency over performance.

12. Asynchronous Circuits: Asynchronous or clockless circuits eliminate the need for a global clock signal and can be more power-efficient for certain applications, although they can be more complex to design and verify.

13. Energy-Efficient Algorithms: Implement energy-efficient algorithms and data processing techniques that minimize computational requirements and memory access.

14. Duty Cycling: In applications like wireless communication, duty cycling involves turning on the radio or transmitter only when data needs to be sent or received, allowing the circuit to spend more time in low-power modes.

15. Energy Harvesting: In some cases, energy can be harvested from the environment to power CMOS circuits, reducing the reliance on traditional power sources.

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3. Methods

SL.NO	AUTHOR	TITLE	YEAR	CONCEPT	METHOD
1	G.SARANYA, R.S. KIRUTHIKA	OPTIMIZED DESIGN OF AN ALU BLOCK USING ARCHITECTURAL LEVEL OF POWER OPTIMIZATION TECHNIQUES	Mar-11	ALU POWER REDUCTION	POWER GATING
2	ADITI SHINDE,VISHWANI D AGRAWAL	MANAGING PERFORMANCE & EFFICIENCY OF A PROCESSOR	Jan-13	PROCESSOR PERFORMANCE	CHARACTERIZATION in terms of f vs η vs Vdd

3	N.RAVINDRAN,R.MARY LOURDE	AN OPTIMUM VLSI DESIGN OF 16-BIT ALU	Mar-15	ALU POWER REDUCTION	MIXED LOGIC
4	GUANG-MINGTANG, KENSUKE TAKATA	4-BIT SLICE ALU FOR 32-BIT RSFQ MICROPROCESSORS	Jan-16	ALU FOR MIPS32 INSTRUCTION SET	SYNCHRONOUS CONCURRENT FLOW CLOCKING
5	JINHUI WANG, NA GONG	PNS-FCR:FLEXIBLE CHARGE RECYCLING DYNAMIC CIRCUIT TECHNIQUE FOR LOW POWER MICROPROCESSORS	Feb-16	HIGHER POWER EFFICIENCY	P-TYPE/N-TYPE DYNAMIC CIRCUIT SELECTION ALGORITHM& FCR
6	YU-GUANG CHEN,WAN-YU WEN	A NOVEL LOW COST DYNAMIC LOGIC RECONFIGURABLE STRUCTURE STRATEGY FOR LOW POWER OPTIMIZATION	Aug-16	EXTENSION OF DYNAMIC VOLTAGE FREQUENCY SCALING(DVFS)	DLRS: DYNAMIC LOGIC RECONFIGURABLE STRUCTURE
7	CHRISTOPHER SCHAEF, JASON T STAUTH	EFFICIENT VOLTAGE REGULATION FOR MICROPROCESSOR CORES STACKED IN VERTICAL VOLTAGE DOMAINS	Feb-16	EFFICIENT VOLTAGE REGUALTION	POWER CONVERSION TOPOLOGY TO MULTICORE REGULATION
8	LAWRENCE T.CLARK, DAN W. PATTERSON	AN EMBEDDED MICROPROCESSOR RADIATION HARDENED BY MICROARCHITECTURE & CIRCUITS	Feb-16	RADIATION HARDENED BY DESIGN EMBEDDED MICROPROCESSOR	MINIMIZATION OF PERFORMANCE REDUCTION FROM HARDENING
9	CHENG-YEN LEE,PING-HSUAN HSIES	A STANDARD CELL DESIGN FLOW COMPATIBLE ENERGY RECYCLING LOGIC WITH 70% ENERGY SAVING	Jan-16	LOW POWER	ENERGY RECYCLING MICROARCHITECTURE & ADIABATIC LOGIC

10	AN-TAI XIAO,YUNG-SIANG MIAO	A VARIABLE VOLTAGE LOW POWER TECHNIQUE FOR DIGITAL CIRCUIT SYSTEM	Mar-16	LOW POWER	VOLTAGE FREQUENCY ADJUSTOR (VFA) & FREQUENCY DUTY CYCLE ADJUSTOR(FDCA) CIRCUITS
11	HAKONTOREYIN,PAMELAT BHATTI	A LOW POWER ASIC SIGNAL PROCESSOR FOR A VESTIBULAR PROSTHESIS	Jun-16	LOW POWER PROCESSOR	COORDINATE SYSTEM TRANSFORMATION TO CORRECT FOR MISALIGNMENT BETWEEN NATURAL SENSORS & IMPLANTED INERTIAL SENSORS
12	SMITA SINGHAL,NIDHI GAUR	ANALYSIS & COMPARISION OF LEAKAGE POWER REDUCTION TECHNIQUES IN CMOS CIRCUITS	Sep-15	LEAKAGE POWER REDUCTION TECHNIQUES	MULTI-THRESHOLD CMOS, SUPER-CUTOFF CMOS,ZIGZAQ, STACK EFFECT,LECTOR,SLEEPY STACK,SLEEPY KEEPER,DUAL SLEEP,SLEEPY-PASS GATE & TRANSISTOR GATING
13	JEFFERSONA HORA,NIEVAM MAPULA	DESIGN OF RF TO DC CONVERTER IN 90NM CMOS TECHNOLOGY FOR ULTRA LOW POWER APPLICATION	Dec-15	ULTRA LOW POWER	VOLTAGE RECTIFIER IS USED
14	MANAS SINGHAL,RAJESH MEHRA	LAYOUT DEVELOPMENT OF AREA EFFICIENT LO-SKEWED EVEN PARITY GENERATOR	Dec-15	AREA EFFICIENCY	UNSKEWED & LOSKEWED TECHNIQUES

15	ANDRES GOMEZ,CHRISTIAN PINTO	REDUCING ENERGY CONSUMPTION IN MICROCONTROLLER-BASED PLATFORMS WITH LOW DESIGN MARGIN CO-PROCESSORS	Oct-15	ENERGY MINIMIZATION TECHNIQUES	DVFS,THERMAL MANAGEMENT TECHNIQUES
16	SARANG KULKARNI,NEHA RAI	A 0.25µm SCVL BASED 4T DRAM DESIGN FOR MINIMIZING LEAKAGE CURRENT USING CMOS TECHNOLOGY	Sep-15	MINIMIZING LEAKAGE CURRENT	SELF CONTROLLABLE VOLTAGE LEVEL TECHNIQUE
17	XIAOZHE LIU, YONGAN ZHENG	AN ULTRA LOW POWER DIGITAL PROCESSOR FOR CHINESE UHF RFID TRANSPONDER	Oct-15	LOW POWER BASE BAND PROCESSOR FOR UHF RFID TAG	HIGHLY REUSED REGISTER BANK , LOW FRQUENCY DECODING & SORT ALGORITHM
18	R VANITHA,S.THENMOZHI	LOW POWER CMOS COMPARATOR USING BIPOLAR CMOS TECHNOLOGY FOR SIGNAL PROCESSING APPLICATIONS	Aug-15	ADC	SUPPLY BOOSTING,BODY-DRIVEN TRANSISTORS, CURRENT MODE DESIGN
19	JENIL,RAHUL	DESIGN & DEVELOPMENT OF EFFICIENT REVERSIBLE FLOATING POINT ARITHMETIC UNIT	Nov-15	REVERSIBLE FPAU	REVERSIBLE LOGIC,QUANTUM CIRCUIT
20	TOMOKI, SHINTARO	A LOW POWER 6T-4C NON VOLATILE MEMORY USING CHARGE SHARING & NON-PRECHARGE TECHNIQUES	Mar-15	FRAM	BITLINE NONPRECHARGE TECHNIQUE, PLATE LINE CHARGE SHARE TECHNIQUE
21	G KARTHIK REDDY	LOW POWER PASS TRANSISTOR LOGIC BASED ALU DESIGN USING LOW POWER FULL ADDER DESIGN	Mar-15	ALU DESIGN	PASS TRANSISTOR LOGIC

22	JAGADEEP KAUR, SHIWANI	DESIGN OF FULL ADDER CIRCUIT USING DOUBLE GATE MOSFET	Oct-15	FULL ADDER	DOUBLE GATE PTL
23	BALAMURUGAN V	PERFORMANCE ANAYSIS OF ASYNCHRONOUS DUAL MODE LOGIC USING LEAKAGE POWER REDUCTION TECHNIQUES	Jun-15	DYNAMIC POWER & LEAKAGE POWER	DUAL MODE LOGIC APPROACH
24	DANIEL,ALEXANDER	INTRA-OPERATION DYNAMIC VOLTAGE SCALING	Apr-15	VOTAGE SCALING	INTRA OPERATION DYNAMIC VOLTAGE SCALING
25	HIPPOLYTE, BHEKISIPHO	LEAKAGE CURRENT MINIMISATION & POWER REDUCTION TECHNIQUES USING SUB-THRESHOLD DESIGN	Mar-15	LEAKAGE POWER REDUCTION TECHNIQUES	SUBTHRESHOLD DESIGN
26	VARSHA BENDRE,DR A.K.KURESHI	AN OVERVIEW OF VARIOUS LEAKAGE POWER REDUCTION TECHNIQUES IN DEEP SUBMICRON TECHNOLOGIES	Nov-15	LOW POWER	DTCMOS,VTMOS,MTCMOS,SCCMOS,FORCED STACKING,SLEEPY KEEPER ,LECTOR
27	BYUNG-DO,YANG	LOW-POWER & AREA EFFICIENT SHIFT REGISTER USING PULSED LATCHES	Jun-15	LOW POWER & AREA EFFICIENT	PULSED LATCHES
28	YUAN CAO, LE ZHANG	A LOW POWER HYBRID RO PUF WITH IMPROVED THERNAL STABILITY FOR LIGHTWEIGHT APPLICATIONS	Jul-15	RING OSCILLATOR PHYSICAL UNCLONABLE FUNCTION	DYNAMIC VARIATION OF OSCILLATION FREQUENCY

29	JOSE,JENS	AN ULTRA LOW POWER MIXED SIGNAL BACK END FOR PASSIVE SENSOR UHF RFID TRANSPONDERS	Feb-12	BASE BAND PROCESSOR, PASSIVE SENSOR	MIXED SIGNAL BACK END FO UHF SENSOR RFID
30	ANGSHUMAN,SAMBHU	A TECHNIQUE FOR POWER REDUCTION OF CMOS CIRCUIT AT 65nm TECHNOLOGY	Jun-12	POWER CONSUMPTION	TRANSISTOR STACKING TECHNIQUE
31	LIANGBO XIE,JIAXIN	A LOW POWER BASEBAND PROCESSOR WITH CLOCK VARIANCE-TOLERANT FOR UHF RFID TRANSPODER	Jan-13	BASE BAND PROCESSOR	CLOCK VARIANCE TOLERANT
32	JIN-FA LIN	LOW POWER PULSE-TRIGGERED FLIP-FLOP DESIGN BASED ON A SIGNAL FEED THROUGH SCHEME	Jun-13	FLIP FLOP	PULSE TRIGGERD FLIP FLOP
33	YA-TING,JAI-MING	EFFECTIVE & EFFICIENT APPROACH FOR POWER REDUCTION BY USING MULTI BIT FLIP FLOPS	Apr-13	MULTI BIT FLIP FLOP	FLIP FLOPS MERGE
34	PER LARSON, KJELL JEPPSON	TIMING & POWER DRIVEN ALU DESIGN TRAINING USING SPREADSHEET-BASED ARITHMETIC EXPLORATION	Jun-14	ALU DESIGN	SPREAD SHEET DESIGN
35	LENIN,NORS YAHIRA	DESIGN & SYNTHESIS OF REVERSIBLE ALU	Sep-14	ALU DESIGN	PERES GATES
36	NA GONG,JIMHUI WANG	APPLICATION DRIVEN POWER EFFICIENT ALU DESIGN METHODOLOGY FOR MODERN MICROPROCESSORS	Jun-13	ALU DESIGN	PNSA

37	VIBHU SHARMA	MINIMUM CURRENT CONSUMPTION TRANSISTION TIME OPTIMIZATION METHODOLOGY FOR LOW POWER ASPECTS	Sep-13	LOW POWER	OPTIMIZATION METHODOLOGY
38	Patanjali Prakash, Saxena	Design of Low Power High Speed ALU Using Feedback Switch Logic	Sep-14	ALU DESIGN	FEEDBACK SWITCH LOGIC
39	Anu Tonk, Shilpa Goyal	A Literature Review on Leakage and Power Reduction Techniques in CMOS VLSI Design	Feb-15	Literature Review on leakage power reduction techniques	MTCMOC,DUAL VT,FORCED STACK,ZIGZAG,SLEEPY STACK,SLEEPY KEEPER,LEAKAGE FEEDBACK,LECTOR,GALEOR,LECTOR stackstateretention
40	Anja Niedermeier, Kjetil Svarstad	The Challenges of Implementing Fine Grained Power Gating	May-10	LOW POWER	POWER GATING
41	Sin-Yu Chen,Rung-Bin Lin	Power Gating Design for StandardCell-Like Structured ASICs	Mar-10	LEAKAGE POWER REDUCTION	POWER GATING
42	Hossein Aghabada, Student Member	Static Power Optimization of a Full-Adder under Front -End of Lne Systematic Variations	Jan-09	STATIC POWER OPTIMIZATION	LEAKAGE AWARE OPTIMIZATION
43	A.Sathanuri, A.Calimera	On Quantifyin the Figures of Merit of Power-Gatin for Leakage Power	May-08	Power Gating	Investigations of the Figure of Merit for power

		Minimization in Nanometer CMOS Circuits			gating
44	Kimiyoshi Usami,Naoki Ohkubo	A Design Approach for Fine-grained Run-Time Power Gating using Locallu Extracted Sleep Signals	Jan-06	Design methodology for power gating	POWER GATING in a Fine grained manner
45	Hailin Jian,Malgorzata Marek-Sadowska	Benefits and Costs of Power-Gating Techniques	Mar-05	Power Gating	sleep transistor sizing, decap insertion
46	Zhigang Hu,Alper Buyuktosunoglu	Microarchitectural Techniques for Power Gating of Execution Units	Aug-04	power Gating	power gate fixed point units
47	James B.Kuo	Evolution of Low-Voltage CMOS Digital VLSI Circuits Using Bootstrap Techniques	Jan-04	LOW POWER	low voltage cmos digtal vlsi circuits
48	Daniel SC Kwok ,Martin Margala	Optimization Techniques For Maximum Power-Efficiency of Deep Sub-Micron CMOS Digital Circuits	May-00	Maximum power efficiency	cmos digital circuits optimization techniques
49	Hendrawan Soelman,Kaushik Roy	Estimating Circuit Activity in Combinational CMOS Digital Circuits	Aug-00	Circuit activity factor	Fast & accurate probabilistic & statistical techniques for estimating circuit activity factor
50	J.Adam Butts ,Gurindar S.Sohi	A Static Power Model for Architects	Jan-00	STATIC POWER OPTIMIZATION	static power models forarchitects

51	Beom Seon Ryu,Hyoung Sok Oh	Multilevel Approaches to Low power 16Bits ALU Design	Feb-99	LOW POWER DESIGN	Multilevel approaches of ALU's
52	Mark C Johnson,Dinesh Somasekhar	Leakage Control With Efficient Use of Transistor Stacks in Single Threshold CMOS	Feb-99	LEAKAGE CONTROL	EFFICIENT USE OF TRANSISTOR STACKS
53	Qi Wang,Sarma	Static Power Optimization of Deep Submicron CMOS Circuits for Dual VT Technology	Jan-98	STATIC POWER OPTIMIZATION	DUALVT TECHNOLOGY
54	Farid N.Nahm	Low-Power Design Methodology:Power Extimation and Optimization	Mar-97	Design methodology for power gating	POWER ESTIMATION & OPTIMIZATION
55	Thomas D.Buard,Robert W.Brodersen	Energy Efficient CMOS Microprocessor Design	Mar-95	MICROPROCESSOR DESIGN	ENERGY EFFICIENT TECHNIQUES
56	William Athas	The Design and Implementation of a Low - Power Clock-Powered Microprocessor	Nov-00	LOW POWERED CLOCK SYSTEM	IMPLEMENTATION OF CLOCK SYSTEM FOR MICROPROCESSOR
57	Takayasu Sakurai	Alpha-Power Law MOSFET Model and its Applications to CMOS Inverter Delay and Other Formulas	Apr-90	CMOS INVERTER DELAY	ALPHA POWER LAW MODEL
58	JD Warnock,JM Keaty	The circuit and physical design of the POWER4 microprocessor	Jan-02	POWER4 MICROPROCESSOR	CIRCUIT DESIGN OF MICROPROCESSOR

59	Andrew S.Hwang	Radiation Hardened 32-bit RISC Microprocessor	Mar-00	MICROPROCESSOR DESIGN	RADIATION HARDEND 32-BIT
60	Sang-Won Lee,Yun-Seob Song	Raptor: A Single Chip Multiprocessor	May-99	MULTIPROCESSOR	RAPTOR SINGLE CHIP PROCESSOR
61	Jack Choquette,Mayank Gupta	High-Perfprmance RISC Microprocessors	Feb-99	RISC PROCESSOR	HIGH PERFORMANCE RISC PROCESSOR DESIGN
62	Macro Antonio Simon Dal Poz,Jose Edinson Aedo Cobo	A Simple Risc Microprocessor Core Designed for Digital Set-Top-Box Applications	Mar-00	SET TOP BOX PROCESSOR	RISC PROCESSOR COR FOR DIGITAL STB APPLICATIONS
63	Tukka Kasanko,Jari Nurmi	Verfication of a 32-bit RISC Processor Core	Jan-04	RISC CORE PROCESSOR	VERIFICATION OF A 32-BIT PROCESSOR
64	Tukka Kasanko,Jari Nurmi	Functional Verfication of a 32-bit RISC Processor Core	Jan-04	RISC CORE PROCESSOR	FUNCTIONAL VERIFICATION OF A 32-BIT PROCESSOR

66	G.Russell i.D. Elliott	Design of Highly Reliable VLSI Processor Incorporating Concurrent Error Detection/Correction	Mar-91	HIGHLY RELIABLE VLSI PROCESSOR	CONCURRENT ERROR DETECTION/CORRECTION
67	Craig Gleason,Mark Forsyth	CMOS Processor Circuit Design in Hewlett-Packard's Series 700 Workstations	Mar-91	CMOS PROCESSOR DESIGN	PROCESSOR DESIGN IN HP SERIES 700 WORKSTATIONS
68	Mitsuru Hiraki,Ramind er S	Stage-Skip Pipeline: A Low Power Processor Architecture Using a Decoded Instruction Buffer	Mar-96	LOW POWER PROCESSOR	STAGE SKIP PIPELINE ARCHITECTURE USING DECODED INSTRUCTION BUFFER
69	Airul Azha Abd Rahman, Zainol Abidin Abdul Rashid	The Pesona16tm RISC 16-Bit Microprocessor-Architecture,Functional Configurations, and Performances	Jan-00	PESONA 16TM RISC PROCESSOR	PROCESSOR FUNCTIONAL CONFIGURATION & PERFORMANCES
70	P.D Hyde, ,G.Russell	A Comparative Study of the Design of Synchronous and Asynchronous Self Checking RISC Processors		DESIGN OF SYNCHRNOUS & ASYNCHRONOUS SELF CHECKING RISC PROCESSORS	COMPARATIVE STUDY ANALYSIS OF SYNCHRONOUS &ASYNCHRONOUS RISC PROCESSOR
71	Scott Davidson	An insider's look at microprocessor design	Mar-06	MICROPROCESSOR DESIGN	ARCHITECTURE & INDEPTH ANALYSIS OF PROCESSOR DESIGN
72	Seung Pyo Jung, Kang-joo Kim	Design & Verification of 16 Bit RISC Processor	Jan-08	16-BIT RISC PROCESSOR	DESIGN & VERIFICATION OF 16-BIT PROCESSOR

73	Blaine Stackhouse, Sal Bhimji	A 65 nm 2-Billion Transistor Quad-Core Itanium Processor	Jan-09	QUAD CORE ITANIUM PROCESSOR	TECHNOLOGY DEPENDENT QUAD CORE PROCESSOR DESIGN
74	Georgios K Konstadinidis	Challenges in Microprocessor Physical and Power Management Design	Jan-09	MICROPROCESSOR DESIGN PROBLEMS	PROBLEMS IN PHYSICAL & POWER MANAGEMENT DESIGN
75	S. Merniz,M.Benmohammed	A Scalable Proof Methodology for RISC Processor Designs A Functional Approach	Jan-08	RISC PROCESSOR DESIGN	SCALABLE METHODOLOGY FOR RISC PROCESSOR DESIGN
76	Xiao Tiejun,Liu Fang	16-Bit Teaching Microprocessor Design and Application	Mar-08	MICROPROCESSOR DESIGN	16-BIT PROCESSOR DESIGN & APLLICATIONS
77	Hongzhong Zheng	Power and Performance Trade-Offs in Contempory DRAM System Designs for Multicore Processors	Aug-10	MULTICORE PROCESSORS	POWER & PERFORMANCE TRADE-OFFs IN DRAM SYSTEM DESIGNS OF MULTICORE PROCESSORS
78	Naghmeh Karimi	Workload-Cognizant Concurrent Error Detection in the Scheduler of a Modern Microprocessor	Sep-11	MODREN MICROPROCESSOR	CONCURRENT ERROR DETECTION IN SCHEDULER OF A MICROPROCESSOR
79	Haitong Tian,Wai-Chung Tang	Postgrid Clock Routing for High Performance Microprocessor Designs	Feb-12	HIGH PERFORMANCE MICROPROCESSOR DESIGN	POSTGRID CLOCK ROUTING PROCESSOR DESIGN

80	Po-Lin Chiu	Interpolation-Based QR Decomposition and Channel Estimation Processor for MIMO-OFDM System	May-11	CHANNEL ESTIMATION PROCESSOR	INTERPOLATION based QR Decomposition PROCESSOR DESIGN for MIMO-OFDM SYSTEM
81	Saulo O.D Luiz	System Identification and Energy-aware Processor Utilization Control	Feb-12	MICROPROCESSOR DESIGN	SYSTEM IDENTIFICATION & ENERGY AWARE UTILIZATION CONTROL OF PROCESSOR
82	Andrew B Kahng	Recovery-Driven Design:Exploiting Error Resilience in Design of Energy-Efficient Processors	Mar-12	PROCESSOR PERFORMANCE	ENERGY EFFICIENT TECHNIQUES
83	Na Gong	TM-Rf: Aging-Aware Power-Efficient Register File Design for Modern Microprocessors	Jul-15	HIGH PERFORMANCE MICROPROCESSOR DESIGN	AGING AWARE POWER EFFICIENT REGISTER FILE DESIGN FOR MODREN MICROPROCESSORS
84	Aditi Shinde,Vishwani D.Agrawal	Managing Performance and Efficiency of a Processor	Mar-13	MICROPROCESSOR PERFORMANCE	TECHNIQUES TO MANAGE PERFORMANCE & EFFICIENCY OF MICROPROCESSOR
85	Michael Bauer,Daniel Lohn	Design and Evaluation of an Adaptive Real-time Microprocessor	Jan-13	ADAPTIVE REAL TIME MICROPROCESSOR	DESIGN & VERIFICATION OF REAL TIME ADAPTIVE PROCESSOR
86	PVS Bharadwaja, K Ravi Teja	Advanced Low Power RISC Processor Design using MIPS Instruction Set	Sep-15	LOW POWER DESIGN	RISC PROCESSOR USING MIPS INSTRUCTION

					SET
87	Mohit N.Topiwala,N. Saraswathi	Implementation of a 32-bit MIPS Based RISC Processor using Cadence	Jan-14	MICROPROCESSOR DESIGN	IMPLEMENTATION OF32-BIT MICROPROCESSOR USING CADENCE
88	C.B. Hsu,J B Kuo	Power Consumpition Optimization Methodology (PCOM) for Low-Power/Low-Voltage 32-bit Microprocessor Circuit Desing via MTCMOS	Jan-14	LOW POWER DESIGN	32-BIT MICROPROCESSOR CIRCUIT DESIGN USING MTCOMS
89	Daniel Lohn, Michael Bauer	Design and Evaluation of an Energy-saving Real-time Microprocessor	Mar-14	LOW POWER DESIGN	DESIGN OF ENERGY SAVING TECHNIQUES FOR MICROPROCESSOR
90	Tiago Reimann	Gate Sizing and Threshold Voltage Assignment for High Performance Microprocessor Designs	Mar-15	HIGH PERFORMANCE MICROPROCESSOR DESIGN	DESIGN OF HIGH PERFORMANCE PROCESSOR USING GATE SIZING &THRESHOLD VOLTAGE ASSIGNMENTS
91	Priyanka Trivedi,Raja prasad Tripathi	Design & Analysis of 16 bit RISC Processor Using low power Pipelining	Mar-15	LOW POWER PROCESSOR DESIGN	ANALYSIS & DESIGN OF 16-BIT PROCESSOR USING PIPELINING TECHNIQUE
92	vazen melikyan,Davit Babyan	Clock Gating and Multi-Vth Low power design methods Based on 32/28 nm ORCA Processor	Jan-15	LOW POWER PROCESSOR DESIGN	CLOCK GATING & MULTI THRESHOLD VOLTAGE DESIGN METHODS FOR

					ORCA PROCESSOR
93	Narender Kumar, Munish Rattan	Implementation of Embedded RISC Processor with Dynamic Power Management for Low-Power Embedded system on SOC	Dec-15	LOW POWER EMBEDDED SOC	DYNAMIC POWER MANAGEMENT FOR RISC PROCESSOR
94	Awais Yousaf,Shahid Masud	Stochastic Model based Dynamic Power Estimation of Microprocessor using Imperas Simulator	Jan-16	POWER ESTIMATION OF MICROPROCESSOR	DYNAMIC POWER CALCULATION USING STOCHASTIC MODEL IMPERAS SIMULATOR
95	Jae Woong Chun , C. Y. Roger Chen	A novel leakage power reduction technique for CMOS circuit design	Jan-10	LEAKAGE POWER REDUCTION TECHNIQUES	DRAIN GATING VARIATIONS
96	HeungJun Jeon, Yong - Bin Kim	Standby leakage power reduction technique for nanoscale CMOS VLSI systems	May-10	LEAKAGE POWER REDUCTION TECHNIQUES	FOR NANOSCALE VLSI SYTEMS STANDYBY LEAKAGE POWER REDUCTION
97	Carlos Ortega, Jonathan Tse,Rajit Manohar	Static power reduction techniques for Asynchronous Circuits	Mar-10	LOW POWER TECHNIQUES	STATIC POWER REDUCTION TECHNIQUES FOR ASYNCHRONOUS CIRCUITS
98	Anmol Mathur, Qi Wang	Power Reduction Techniques and Flows at RTL and Sytem Level	Feb-09	POWER REDUCTION TECHNIQUES	SYSTEM LEVEL POWER REDUCTION TECHNIQUES

99	Stefan Rusu, Simon Tam,Harry Muljono	Power reduction technique for an 8 core Xeon processer	Mar-09	POWER REDUCTION TECHNIQUES	8 CORE XEON PROCESSOR POWER REDUCTION TECHNIQUES
100	Bo Zhai,Sanjay Pant, Leyla Nazhandali	Energy efficient subthreshold processor design	Jun-09	LOW POWER PROCESSOR DESIGN	EFFICIIENT SUBTHRESHOLD MICROPROCESSOR DESIGN
101	Patanjali Prakesh & Saxena	Design of Low High Speed ALU using feedback Switch Logic	Nov-09	ALU DESIGN	FEEDBACK SWITCH LOGIC FOR LOW POWER HIGH SPEED ALU
102	Jose A. RODriguez, Jens Masuch Woong Chun , C. Y. Roger Chen	An EPC Class-1 Generation-2 Basedband Processor for passive UHF RFID Tag	Dec-09	BASEBAND PROCESSOR DESIGN	EPC CLASS PROCESSOR FOR PASSIVE UHF TAGS
103	Andrea, Grisanti	Improved Pervasive Sensing with RFID: An ultra low power baseband Processor for UHF Tags	Dec-09	BASEBAND PROCESSOR DESIGN	AN ULTRA LOW POWER BASEBAND PROCESSOR DESIGN
104	Lee,Seok	Standby leakage power reduction technique for ultra low power processors	Dec-08	ULTRA LOW POWER	STANDBY LEAKAGE POWER REDUCTION TECHNIQUE FOR PORCESSOR DESIGN
105	Yu Zhou, Hui Guo	Application Specfic power ALU design	Mar-08	ALU DESIGN	APPLICATION SPECFIC LOW POWER ALU DESIGN

106	Nishimura,Hirai,Saito	Power Reduction Techniques for dynamically reconfigurable processor arrays	Jun-08	RECONFIGURABLE PROCESSOR ARRAYS DESIGN	LOW POWER REDUCTION TECHNIQUES FOR RECONFIGURABLE PROCESSOR ARRAYS
107	Vahid,Vali,Siamak	A Low Power baseband processor for a dual mode UHF EPC Gen 2 RFID tags	Sep-08	BASEBAND PROCESSOR DESIGN	LOW POWER PROCESSOR FOR DUAL MODE EPC RFID TAGs
108	Jansuz,Haibo	A Novel low power circuit design scheme	Feb-07	LOW POWER DESIGN	NOVEL CIRCUIT DESIGN TECHNIQUE FOR LOW POWER
109	Vasily,Moshnyaga	Power reduction techniques for digital array multipliers	Jun-07	DESIGN OF DIGTAL ARRAY MULTIPLIERS	VARIOUS POWER REDUCTION TECHNIQUES FOR ARRAY MULTIPLIERS
110	Philippe,Hugh, Franck	Leakage Power reduction techniques applied to 90 nm SoC application processor	Feb-06	DESIGN OF APPLICATION SPECFIC PROCESSOR	LEAKAGE POWER REDUCTION TECHNIQUES FOR SoC
111	H Peter Hoftstee	Power Efficient Processor Architecture & the cell processor	Jan-05	DESIGN OF CELL PROCESSOR	POWER EFFICIENT ARCHITECTUREs FOR CELL PROCESSOR DESIGN
112	Michael J Flynn, PatricHung	Microprocessor Design Issues: Thoughts in the road ahead	Jun-05	MICROPROCESSOR DESIGN	VARIOUS POWER REDUCTION TECHNIQUES & THEIR ISSUES IN PROCESSOR

113	Alice Wang, Anantha Chandrakasan	A 180-mv Subthreshold FFT Processor using a minimum energy design methodolgy	Jan-05	FFT PROCESSOR DESIGN	SUBTHRESHOLD DESIGN OF FFT PROCESSOR USING MINIMUM ENERGY TECHNIQUE
114	Mohamed,Fahim	Robust & Efficient dynamic voltage scaling architecture	Jan-03	VOTAGE SCALING	EFFICIENT TECHNIQUES FOR DYNAMIC VOLTAGE SCALING
115	Jaewon, Massoud	Gated Clock routing for low power microprocessor design	Jun-01	MICROPROCESSOR DESIGN	LOW POWER MICROPROCESSOR DESIGN USING GATED CLOCK ROUTING
116	Tadahiro Kuroda	Low power high speed CMOS vlsi design	Sep-02	CMOS VLSI CIRCUITS	LOW POWER & HIGH SPEED VLSI DESIGN FOR CMOS CIRCUITS
117	Bill Pontikakis, Mohamed Nekili	A Novel Double Edge Triggered Pulse clock TSPC D FLIP FLOP for high performance & low power VLSI design applications	Jan-02	LOW POWER VLSI DESIGN	DOUBLE EDGE TRIGGRED PULSE CLOCKD FLIP FLOP DESIGN FOR HIGH PERFORMANCE
118	T Devoivre, M Lunenborg	Validated 90 nm CMOS technology platform with low -k copper interconnects for advanced SOC	Mar-02	ADVANCED SoC DESIGN	90NM CMOS TECHNOLOGY WITH LOW -KCOPPER INTERCONNECTS

119	Mahesh,Nikil, Dan	Efficient power reduction techniques for time multiplexed address buses	Oct-02	TIME MULTIPLEXED ADDRESS BUSES DESIGN	POWER REDUCTION TECHNIQUES FOR ADDRESS BUSES. ADDRESS BUS TRANSITION ACTIVITY FOR DRAM'S
120	JinnShyan,Ching Rong,Chingwei	Analysis & Design of high speed & Low Power CMOS PLAs	Aug-01	CMOS PLAs	DESIGN & ANALYSIS OF HIGH SPEED LOW POWER PLAs
121	Thomas, Trevor,Anthony,Robert	A dynamic voltage scaled microprocessor system	Nov-00	MICROPROCESSOR DESIGN	DYNAMIC VOLTAGE SCALING TECHNIQUE PROCESSOR DESIGN
122	Trevor,Thomas,Robert	Voltage Scheduling in the IpARM Microprocessor system	Dec-00	LPARM MICROPROCESSOR SYSTEM	VOLTAGE SCHEDULING IN PROCESSOR SYSTEM
123	Mohamed,Anis	Effect of Technology Scaling on Digital CMOS logic styles	Sep-00	DIGITAL CMOS LOGIC DESIGN	TECHNOLOGY SCALING EFFECTS ON DIGITAL CMOS CIRCUITS
124	Nace,Jennifer,John	An introduction to Plasma etching for vlsi circuit technology	Sep-99	VLSI CIRCUIT TECHNOLOGY	PLASMA TECHNOLOGY INTRODUCTION IN VLSI
125	Richard,Mohamed	Power dissipation analysis & optimization of deep submicron CMOS digital circuits	May-96	CMOS DIGITAL CIRCUITS	ANALYSIS & OPTIMIZATION TECNIQUES FOR POWER IN CMOS DIGITAL CIRCUITS

126	Anantha P. Chandrakasan, Robert	Minimizing Power consumption in Digital CMOS circuits	Apr-95	CMOS DIGITAL CIRCUITS	REDUCING POWER CONSUMPTIO N IN CMOS DIGITAL CIRCUITS
127	Anantha P. Chandrakasan, Robert	Low power CMOSDigital design	Apr-92	CMOS DIGITAL CIRCUITS	VARIOUS TECNIQUES FOR LOW POWER
128	Eric	Low power design: ways to approach the limits	Apr-94	LOW POWER	DIFFERENT APPROACHES FOR OBTAINING LOW POWER
129	Lou Scheffer	CAD tools for microprocessor design in deep submicron ERA	Apr-96	DESIGN FLOW & CAD TOOLS needed to design a modren microprocessor	STRUCTURED CUSTOM DESIGN STYLE
130	Min-Chu Tuan,Shih-Lun Chen	An Efficient micro control unit vlsi design wearable Electronics & Sensor Networks		MICRO CONTROL UNIT DESIGN	EFFICIENT WAY OF MICROCONTR OL UNIT DESIGN FOR SENSORS & WEARABLE ELECTRONICS

4. Results

From the above study & analysis, we can apply majorly for dynamic power consumption, static power consumption reduction techniques along with voltage scaling. Implement low-power states for idle processor cores. The Processor should be able to enter sleep or power-down states when it is not actively executing instructions.Use clock gating at various levels example register files, execution units, to shut down clock signals when not needed.Implement hardware support forDynamic Voltage and Frequency Scaling so that the processor can adapt its voltage and frequency based on workload, further reducing power consumption. For floating-point units,techniques like operand bypassing and low-power floating-point arithmetic units should be used. Minimize power consumption during instruction fetch by using techniques like instruction cache locking or instruction cache partitioning.Use power-efficient branch prediction schemes such as static prediction or selective dynamic prediction to minimize misprediction penalties.Implement a short and efficient pipeline to minimize pipeline stages. A shorter pipeline typically consumes less power as there are fewer clock cycles and stages for data to

traverse. Use aload-store architecture to minimize data movement operations and reduce power consumption. FinFET transistors based processors can be implemented.

5. Discussion

In this paper the various design stratergies and techniques are studied and presented. As microprocessor is revolutioning in current Digital era of IoT & Artificial Intelligence, much attention is needed in research study of minimization techniques for low power, high performance of the electronic devices.

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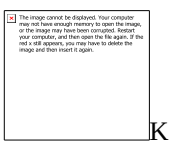

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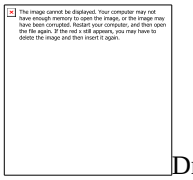

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