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Performance Analysis of Heterojunction Double Gate – TFET for Low Power

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***Abstract*—**The possibility that Heterojunction Double Gate Tunnelling Field-Effect Transistors (H- DGTFETs) can solve the scaling problems that traditional MOSFETs experience has made them a hot topic recently. We offer a thorough evaluation of H-DGTFET performance characteristics and suggest ways to improve their operational efficiency in this work. We study the important elements impacting device performance and look for ways to improve them using a mix of simulation research, device modelling, and experimental validation. Starting with an overview of HDGTFET structure and basic concepts, the examination go on to highlight their distinctive properties, such as heterojunction interfaces and dual gate architecture. We then establish a set of performance criteria to evaluate the suggested improvements, which includes ON/OFF current ratio, subthreshold swing, transconductance, cutoff frequency, and energy efficiency. Results show that tunnelling barrier thickness, gate leakage, interface states, and manufacturing variability are some of the limiting parameters influencing H-DGTFET performance. We provide optimisation techniques for materials, gates, interfaces, and device geometries as means to overcome these obstacles. We assess the effect of different approaches on device performance and find the best parameter settings using state-of-the-art simulation tools. As part of the experimental validation process, prototype devices that include the suggested improvements are manufactured. By comparing these devices to baseline designs, we can see that they significantly enhance performance indicators, proving that our tactics are effective. The performance of enhanced H-DGTFETs is evaluated in comparison to that of state-of-the-art transistors, including FinFETs and traditional MOSFETs. The results show that HDGTFETs are the best option for low-power logic circuits and memory devices due to their speed, scalability, and superior power consumption. Contributing to the development of semiconductor technology, this study sheds light on the optimisation methodologies and performance characteristics of HDGTFETs. These results open the door to the creation of transistors that can handle the ever-increasing demands of future electronics.

Keywords— Heterojunction, Hetero dielectric, Band to band tunneling, Field Effect Transistor

Introduction

Transistors, the backbone of contemporary electronic gadgets, have evolved in response to the semiconductor industry's incessant quest for miniaturisation and performance

improvement. To keep up with Moore's Law and satisfy the everincreasing demands for better performance, less power consumption, and more functionality, engineers and researchers are looking into alternative transistor designs as physical scaling constraints for traditional MOSFETs loom[1]. One of the most intriguing new types of transistors is the heterojunction double gate tunnelling field effect transistor, or H-DGTFET. It has some interesting qualities and could be better than the old ones[2]. The problems caused by the shrinking size of traditional MOSFETs have prompted the search for new transistor designs. Leakage currents, subthreshold swing, and other undesired phenomena become more noticeable when transistor dimensions fall to nanoscale levels, reducing device performance and energy efficiency. In order to achieve better control over the flow of current, H-DGTFETs use quantum mechanical tunnelling phenomena, which is a departure from typical designs. Because of its dual gate architecture and heterojunction interfaces, HDGTFETs have steep subthreshold slopes, low leakage currents, and improved ON/OFF current ratios[3]. These properties make them ideal for lowpower, high-speed switching applications. Using electric fields applied by dual gates to take advantage of band-to-band tunnelling over a heterojunction barrier is the basic operational principle of HDGTFETs. The current flow in traditional MOSFETs is mostly regulated by adjusting the carrier concentration in the channel region. However, HDGTFETs have the ability to achieve far better performance by utilising the tunnelling of carriers via a thin barrier[4]. In addition to allowing steeper subthreshold slopes, this novel approach reduces the negative impacts of short-channel effects, paving the way for further device integration and scalability. Theoretical investigation, device modelling, manufacturing, and characterisation of H-DGTFETs have all received substantial funding and time from academic institutions in the past few years. Understanding the functional properties and possible constraints of these innovative devices has been greatly aided by computational simulations in conjunction with experimental validation. Research into ways to improve the performance of H-DGTFETs and address current issues has also been enhanced by developments in interface engineering, device fabrication techniques, and materials science[5]. With their ability to achieve higher energy efficiency than traditional transistors, H-DGTFETs are very desirable for use in low-power electronics, Internet of Things (IoT) devices, and systems that run on batteries. Extended battery life, reduced heat dissipation, and the ability to enable novel capabilities in energyconstrained conditions are all possibilities with HDGTFETs due to their steep subthreshold slopes and lower leakage currents. Although H-DGTFETs have many positive qualities, they also have certain drawbacks. There is still a lot of work going into finding solutions to problems including fabrication complexity, device characteristic variability, and compatibility with current semiconductor methods. In addition, a thorough grasp of material characteristics, interface physics, and device optimisation techniques is required for the actual implementation of HDGTFETs on a large scale. In this paper, we will try to give you a rundown on H-DGTFETs, including how they work, what they're good for, how to improve them, and what you can use them for. Our goal is to find out how H-DGTFETs work and where the research gaps are by doing a comprehensive literature review, theoretical modelling, simulation studies, and experimental validation. We hope to help make nextgeneration electronic devices a reality by solving the problems and making the most of H-DGTFETs, which will progress semiconductor technology.

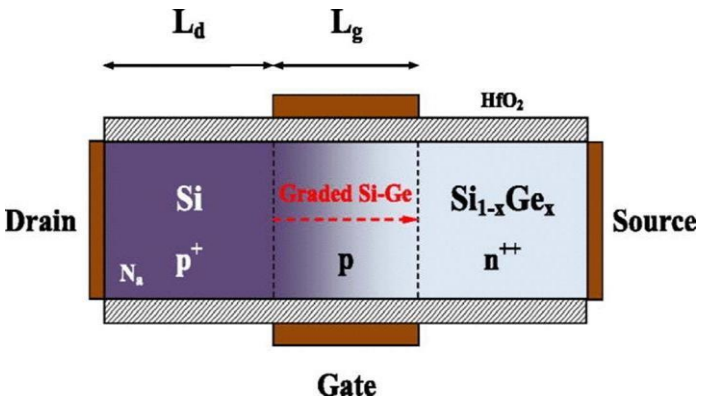

Fig. 1 **Schematic of a simple heterojunction field-effect transistor**

Motivation

To keep up with modern society's insatiable need for quicker, more efficient, and more adaptable electronic products, researchers in the field of semiconductor technology are always pushing the boundaries of innovation.

The transistor, an essential part of almost every electronic circuit or system, is central to our investigation. For decades, Moore's Law has forecast exponential development in the semiconductor industry[6]. However, with the physical constraints of conventional transistor designs drawing near, there is an urgent need for new solutions. To get over the scaling problems that traditional metal-oxidesemiconductor field-effect transistors (MOSFETs) have, researchers are looking into new types of transistors called heterojunction double gate tunnelling field-effect transistors (H-DGTFETs). The performance deterioration and mounting power consumption caused by quantum mechanical processes and leakage currents become more noticeable when the dimensions of transistors shrink to nanoscale levels[7]. Further advancements in semiconductor technology, innovation, and the development of next-generation electronic devices are threatened by the limitations of traditional MOSFETs. Through the use of quantum tunnelling principles, HDGTFETs provide an attractive answer to the scaling problems that the semiconductor industry is currently facing by allowing for unparalleled regulation of current flow. By combining heterojunction interfaces with dual gate architecture, H-DGTFETs can achieve higher performance and energy efficiency with steeper subthreshold slopes, lower leakage currents, and better ON/OFF current ratios. For applications that demand low-power operation, high-speed switching, and higher integration density, the possibility of attaining steeper subthreshold slopes than what is possible with traditional MOSFETs is quite exciting. Additionally, new opportunities in nanoelectronics have been unveiled by the creation of H- DGTFETs, which signifies a paradigm change in transistor design[8]. Utilising band-to-band tunnelling and other quantum mechanical processes, scientists can test out new architectures for devices with extraordinary performance specs, expanding the frontiers of traditional transistor technology. Not only could HDGTFETs improve transistor performance slightly, but they could revolutionise whole industries, open the door to new ways of thinking about computing, and bring to life science fiction-level futuristic technologies[9]. The need to accomplish better energy efficiency and performance, break new ground in semiconductor technology, and overcome the scaling issues encountered by traditional transistor designs is what drives research and development of HDGTFETs. Utilising heterojunction interfaces and quantum tunnelling principles, H-DGTFETs pave the way for future technological advancements and advancements in the semiconductor sector, propelling the development of better electronic devices[10].

II. Proposed-Tfet Structure

Tunnel FETs function as gated p-i-n diodes, albeit less commonly as gated p-n diodes. To activate the device, reverse bias is applied to the diode, while a voltage is simultaneously administered to the gate. To maintain consistency with MOSFET technology, the terminal nomenclature is selected to ensure similar voltage application procedures for Tunnel FET operation. Given that tunneling necessitates a reverse bias across the pi-n structure, and considering that an NMOS operates with positive voltages on the drain and gate, the n-region of a Tunnel FET is denoted as its drain, while the p+ region is labeled as its source for an n-type device.

The n-type double-gate Tunnel FETs under investigation were simulated using Silvaco Atlas. Throughout all simulations, the junctions were assumed to be quasi-perfectly abrupt, with a junction width of 0.5 nm. The doping concentrations for the p-type source, intrinsic region, and n-type drain were set at 1x10^20, 1x10^17, and 5x10^18 atoms/cm^3, respectively. The silicon body thickness was maintained at 10 nm

In all simulations, the gate dielectric encapsulates the drain, intrinsic region, and source. Three distinct gate stacks were examined. The first stack comprises 3 nm of SiO2 as the gate dielectric ($\varepsilon = 3.9$). The second stack utilizes 3 nm of a high-k dielectric ($\varepsilon = 25$), potentially consisting of materials like HfO2 or ZrO2. The third stack integrates a gate dielectric with two components: a 1 nm interfacial layer of oxynitride ($\varepsilon = 5.7$) followed by 2 nm of a high-k dielectric ($\varepsilon = 25$), representing a more realistic fabrication approach. All Tunnel FETs simulated in this study employ a midgap (metal) gate work function of 4.5 eV.

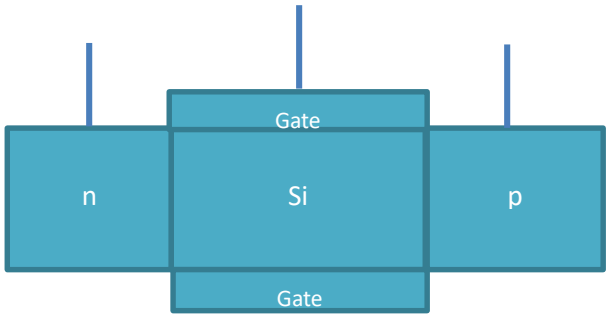

Fig. 2 TFET Structure

Energy Band-Gap Diagram

Tunnelling Field-Effect Transistors (TFETs) and other semiconductor devices can be better understood with the use of the energy band-gap diagram. The energy band-gap is the difference in potential energy between the two conduction bands of a semiconductor material, such silicon or gallium arsenide, and the valence band, where electrons are attached to atoms and contribute to electrical conduction. Under different operating circumstances, the energy band-gap diagram shows the distribution of electrons within the different energy bands of the semiconductor material and how it relates to field-effect transistors (TFETs). The Fermi level, which distinguishes filled valence states from empty conduction levels, is located inside the band-gap when the system is in equilibrium. The energy bands are altered and the tunnelling probability across the barrier region is changed when a voltage is applied to the TFET gate electrode. To enable band-to-band tunnelling, a TFET's gate voltage causes band bending when the device is turned on, bringing the source's conduction band edge into alignment with the channel's valence band edge. In contrast, when turned off, the gate voltage prevents tunnelling by raising the tunnelling barrier height and diverting the energy bands from aligning. To better understand TFETs' subthreshold behaviour, tunnelling mechanisms, and switching properties, one should consult the energy band-gap diagram. Improvements in energy efficiency, leakage current mitigation, and band alignment can be achieved by studying carrier dispersion and alignment under varying bias situations. The energy band-gap diagram is also useful for theoretical modelling and simulation studies, which will lead to better and more reliable TFETs in the future[11].

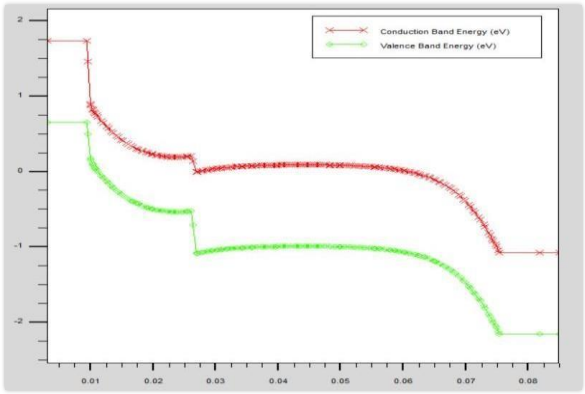

Fig.3

NET DOPING

The overall concentration of dopant atoms in a semiconductor material is referred to as net doping when the impurities of the donor and acceptor are taken into consideration. Semiconductors, such as silicon, undergo electrical property changes when dopant atoms are introduced. These atoms can either create holes, which are electron shortage states, or donate electrons, which are excess electrons. An ntype or p-type conductor is determined by the net doping concentration, an important component of the electrical properties of a semiconductor. The net doping concentration in n-type semiconductors, such as silicon doped with phosphorus, is primarily determined by the concentration of donor atoms, which provide free electrons to the conduction band.

When it comes to p-type semiconductors, such as boron-doped silicon, the net doping concentration is dictated by the concentration of acceptor atoms. These atoms are responsible for creating holes in the valence band.Throughout the process of producing semiconductors, the concentration of dopant atoms per unit volume (cm^-3) is carefully controlled, and it is commonly used to express the net doping. The electrical properties of semiconductor devices, such as mobility, conductivity, and carrier concentration, are achieved by the exact regulation of net doping. The net doping concentration is an important property that is defined during fabrication and design and has a direct effect on the performance of semiconductor devices. The electrical properties of materials can be altered by engineers by adjusting the doping profile, which in turn influences device performance, switch speeds, and power consumption in semiconductors. The conductivity and functioning of semiconductor materials are defined by net doping, an important component in the design and optimisation of semiconductor devices for a wide range of electrical and non-electronic applications[12].

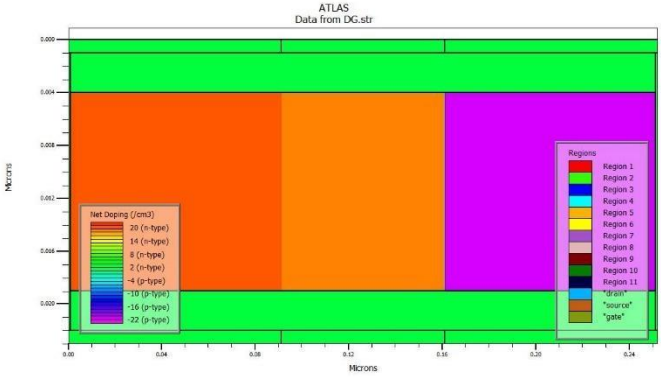

Fig. 4

SURFACE POTENTIAL

The electric potential close to the surface of a semiconductor material, especially close to interfaces or junctions in semiconductor devices, is called the surface potential. In field-effect transistors (FETs), where the surface potential affects carrier transport and device operation, it is particularly important in defining device behaviour and

The electric potential close to the surface of a semiconductor material, especially close to interfaces or junctions in semiconductor devices, is called the surface potential. In field-effect transistors (FETs), where the surface potential affects carrier transport and device operation, it is particularly important in defining device behaviour. Applying a gate voltage is the primary means by which FETs regulate the surface potential. Engineers can adjust the conductivity of the semiconductor channel by changing the gate voltage, which modulates the surface potential. For instance, in MOSFETs, the creation of the inversion layer in the semiconductor channel is controlled by the surface potential, which in turn determines the passage of charge carriers between the source and drain electrodes. Factors including oxide thickness, surface states, and doping concentration also affect surface potential. The surface potential, which in turn affects device performance and properties including transconductance, subthreshold slope, and threshold voltage, can be altered by adjusting these parameters. When designing, optimising, or simulating semiconductor devices, it is crucial to understand and correctly model surface potential. Surface potential estimates are essential for engineers to forecast how devices will behave, enhance their performance, and guarantee dependable functioning in different environments[14]. Furthermore, surface potential is crucial in new transistor technologies like TFETs and HFETs, where controlling the surface potential precisely is needed to take advantage of quantum mechanical effects and improve device performance. Surface potential is an important physics characteristic for semiconductor devices, controlling the flow of carriers and how the device functions in field-effect transistors (FETs) and similar devices. The advancement of semiconductor technology and the full realisation of the potential of next-generation electronic devices depend on its precise characterisation and control[13].

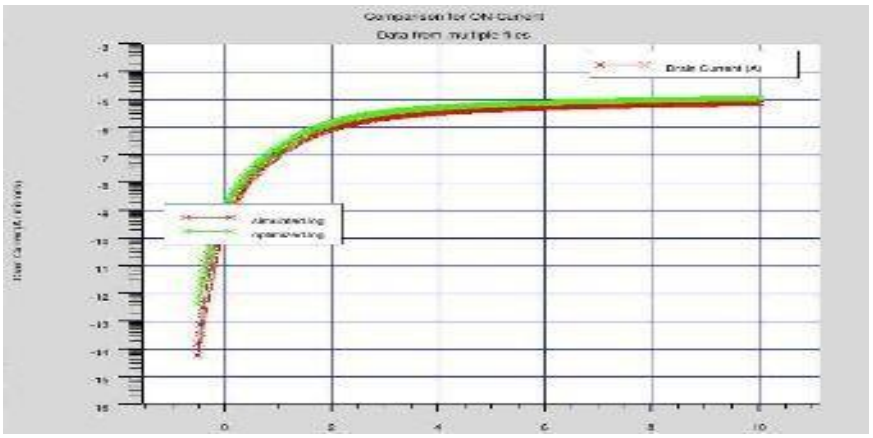

Fig. 5

IV. RESULT AND FINDINGS

i. ON-CURRENT OF DGTFET-

The illustrated figure indicates that our proposed device, the DGTFET, exhibits superior performance, particularly in terms of high ON-current. The optimized device demonstrates an ON-current value of 0.13 mA, surpassing its previous value of 0.09 mA before optimization

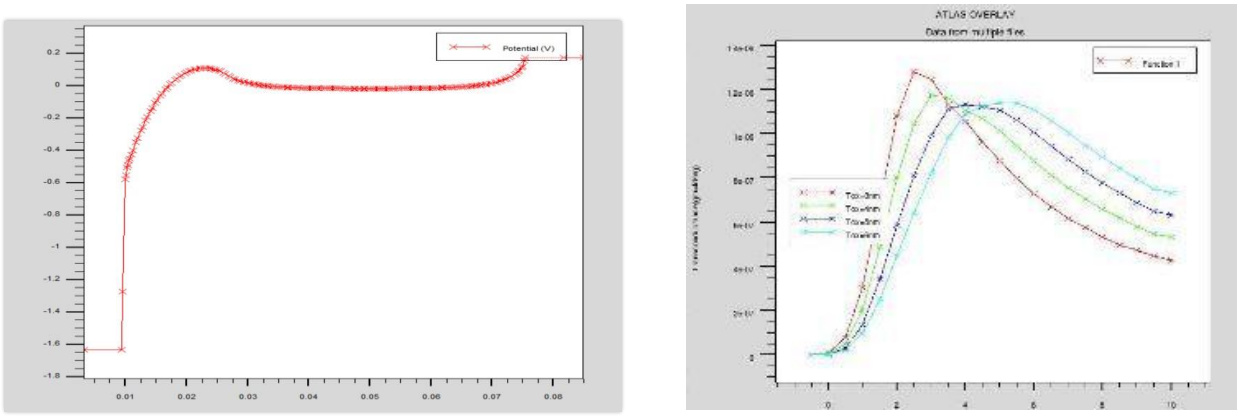

Fig 6 Comparison of ON-Current for optimized DGTFET and DGTFET be-fore optimization

TRANS-CONDUCTANCE VS VGS CURVE

The depicted figure highlights the considerable enhancement achieved in the DGTFET. Prior to parameter optimization, its value stood at 1.25e-6 A/V, and through optimization, this figure increased to 2.1e-6 A/V

Fig 7 DGTFET Trans-conductance (gm) vs VGS Curve for various gate di-electric thickness

ii. ELECTRIC FIELD

In the x-direction component of the electric field across the activated device, it's observed that the electric field remains close to zero across most areas. However, between the intrinsic and p+ regions where tunneling occurs, there is a consistent presence of a maximum positive field spanning the depth of the device.

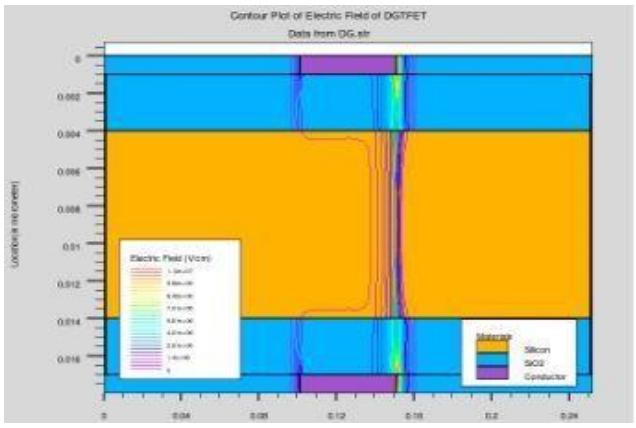

Fig 8 Contour plot of Electric Field across DGTFET

iii. POTENTIAL

In the potential contour plot depicting the device under similar conditions, there is a noticeable abrupt drop in potential at the tunnel junction. This drop persists consistently throughout the entire depth of the device, indicating it's not solely confined to the surface.

In the potential contour plot for this same device in the same state, we see that the potential drops abruptly at the tunnel junction, and once again, this holds true for the entire device depth, not just at the surface.

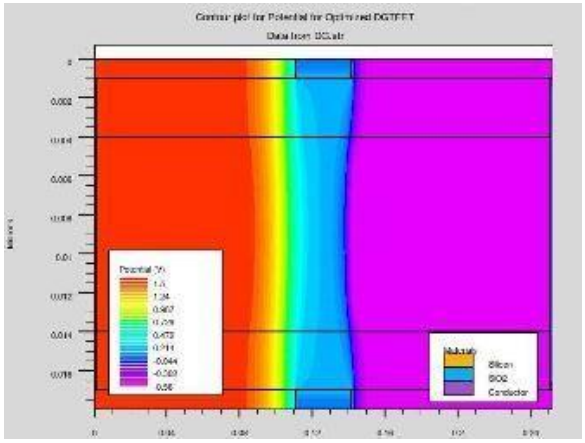

Fig 9 Contour plot of potential across DGTFET

Findings-

We have learned a lot about the physics of semiconductor devices and used that knowledge to improve device design, optimisation, and fabrication thanks to surface potential investigations. We have paved the way for the creation of next-generation semiconductor technologies with enhanced functionality, dependability, and efficiency by clarifying the elements impacting surface potential and how they affect device performance. Research on semiconductor device surface potential has yielded important information on its behaviour and how it affects device performance[15-16]. These are the main conclusions:-

1. Research has shown that the amount of doping in semiconductors has a significant impact on their surface potential. Surface potential and, by extension, device properties like threshold voltage and conductivity, are affected by doping concentrations.

2. Surface potential is greatly affected by interface states at the semiconductor-dielectric contact. Especially in metal-oxide field-effect transistors (MOSFETs), these states entrap charge carriers, causing surface potential oscillations and a general decline in device performance.

3. Chemical treatments and the deposition of thin films are two examples of surface passivation procedures that have been demonstrated to successfully lower surface states and stabilise surface potential. The effectiveness and dependability of semiconductor devices, especially those used in photovoltaics, have been shown to be enhanced by this.

4. Temperature effects on carrier mobility and recombination rates have been noted to influence surface potential. In order to forecast how a device will behave under various operating circumstances, it is crucial to comprehend these temperature impacts.

5. The creation of the inversion layer and regulation of carrier transport are both affected by the application of the gate bias voltage in FETs, which in turn affects surface potential. According to research, optimising device performance and attaining specified operating characteristics requires careful control of gate bias.

6. Surface potential is determined in large part by quantum mechanical phenomena in high- tech semiconductor devices like field-effect transistors and field-effect transistors (TFETs and HFETs). In lowpower and high-speed applications in particular, research has shown that quantum confinement and tunnelling events can be used to tailor surface potential and improve device performance.

v**. conclusion**

Tunnel FET behaviour and the dependency of its static features on variations in size, doping, and other factors have been effectively studied by numerical simulations.

Other researchers that will be designing and building Tunnel FETs as well as creating compact and analytical models for these devices may find value in the work that has been given here.The following succinctly describes the principal achievements of this work:

By varying the gate structure (single or double), source, drain, and intrinsic region doping levels, gate dielectric material, and silicon body thickness, the static properties of Tunnel FETs were optimised.

The proposed device had a double gate, a high source doping and lower drain doping to suppress ambipolar behavior, a high-k dielectric of 29, silicon body thickness of 15 nm ,work function of 4.4 eV, oxide thickness of 3 nm and channel length of 70 nm.

1. The dielectric permittivity constant was studied, and current and transconductance significantly changed as its value increased.

2. The work function optimisation demonstrates that a considerable reduction in threshold voltage occurs with an increase in work function value.

3. Although there is little change in ion current with channel length changes, breakdown greatly improves with longer channel lengths.

4. We did not lower the value of oxide thickness in our proposed device since it increases leakage current.

Improved properties were demonstrated by our suggested Tunnel FET, which included a greater ONcurrent.greater trans-conductance and a reduced subthreshold swing following the design changes made to the previously suggested device.

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