Tuijin Jishu/Journal of Propulsion Technology
ISSN: 1001-4055
Vol. 44 No. 5 (2023)

Implementation of Digital Differentiators using Quantum-dot Cellular Automata

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Abstract:- when it come to scaling of the circuits, the CMOS (Complementary metal-oxide-semiconductor) technology is no longer in the effect, as the semiconductor industry has come up with many number of technologies to reduce the size of the circuit and a single component the technologies has been changed. One of them is the Quantum-dot Cellular Automata. The size of the basic cell used in QCA is in nanometer. Hence by using the Quantum-dot Cellular Automata(QCA) various circuits are designed, here in this work the design of a digital differentiator has been considered. The digital differentiators like First Difference Differentiator, Central Difference Differentiator and the Bilinear Transformation of the IIR filters has been realized. These simple circuits can be further extended to the higher number of bits and be used in the DSP filters. These are realized by using the software QCADesigner, the software used to realize the QCA circuits. By using the arrangement of the cells of the size in terms of nanometers the circuits are designed.

Keywords*: QCA, Differentiator, QCADesigner, CMOS (Complementary metal-oxide-semiconductor).*

1. Introduction

Differentiation in the derivative of the function that is the rate of change of the parameter. For the analog signals the derivative is the slope of the signal as the signal is the continuous. As for the discrete-time signal the slope cannot be determined as well the derivative. There are many number of techniques, which can give the approximate differentiation of the discrete-time signals, where the derivative can be calculated. These are implemented on the hardware, as the differentiation plays a key role in the communication blocks and DSP (Digital Signal Processing) applications. While the hardware implementation currently in the VLSI industry the CMOS (Complementary metal-oxide-semiconductor) has taken the job to complete the task. But scaling of CMOS technology has reached its limit and the need for “Beyond CMOS” devices has arisen[2]. QCA (Quantum-dot Cellular Automata) is one such potential future digital logic technology[3].

The implementation of the circuits can be done in the QCA by using the QCADesigner Software. The QCADesigner is the simulation software the version used in this work is QCADesigner 2.0.3. The simulation is based on the digital values of input.

The concept of QCA was introduced by Dr. C.S Lent and Tougaw in 1993. Quantum dot is the primitive component of QCA technology, the four existing methods of fabricating quantum dots are Semiconductor dots, Metal-islands, Magnetic Dots, and Molecular Dots[3]. The basic block of the QCA is the QCA cell that is of 18nm x 18nm 4-dot cell. The cell consists of 4 quantum dots, each dot has the diameter of 5nm. The cell consist of two free electrons that located in the diagonally opposite locations to avoid coulombic reactions[1]. There are two states of a cell namely unpolarised state and the polarized state. In the polarization state the logic ‘0’ and logic ‘1’ can be represented in Figure 1.

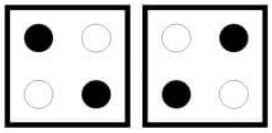


Fig. 1. Polarized QCA cells, the logic 0 and logic 1.

The cell can undergo 4 phases while in the operation there are switch, hold, release and relax. The clocking is application of appropriate voltage to the cell. Clocking leads to the adjustment of tunneling barriers between the quantum dots for transfer of electrons between the dots[4]. In the switch phase the unpolarised cell having the low potential barriers raised, and in the hold phase the barriers are held high. In the release phase the barriers are lowered, and in the relax phase the cell remains in the unpolarised state. The respective phases are shown in Fig.2. The cells can be in 4 clocking zones they are clock0, clock1, clock2, clock3 respectively. Each clock zone is 90^{o} out of phase to each other as shown in Fig.3.

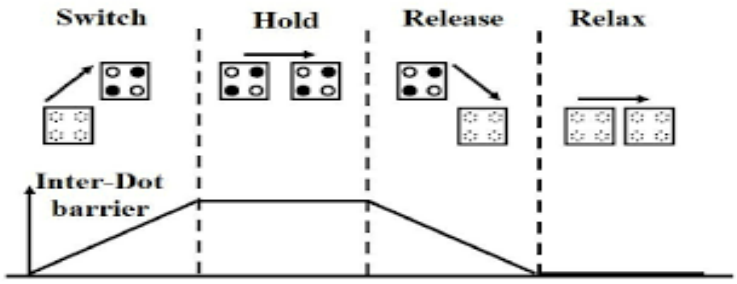


Fig. 2. Phases of the QCA cell while operation.

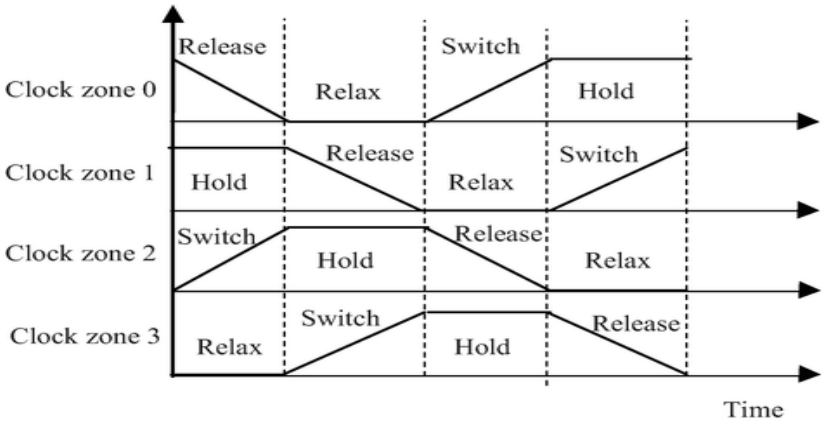
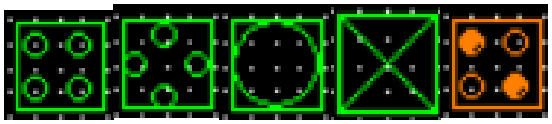


Fig.3. Clock Zones of the QCA cells.

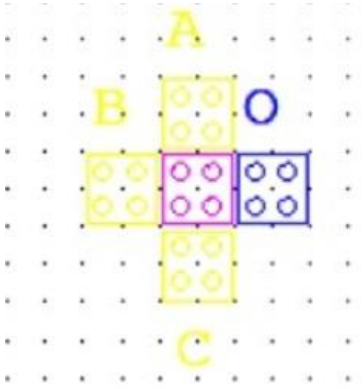
In QCA the circuit may be of single layered and multilayered. In the multi layer the QCA signal should be transfer to other layer, hence the vertical cells are used. The types of cells used in QCA are normal cells, rotated cells, fix polarization cells, vertical cells and cross over cells. Fig4 shows the types of cells and all the cells can be used in the four phases. The normal cell(Fig 4(a)) can be used with any of the clock in the entire circuit also the stability of the signal can be achieved only with the many number of cells, in an example the phase connected to the following circuit may be out of two or three phases apart then we can delay the signal and use all the clocks till the following circuit but all the clocks with single cell cannot give the better results hence for stability of the signal two or more number of cells should be used. In Fig 4(b) the rotated cell is shown, the cell is rotated to 45^{o} also works as the normal cell and all the properties can be applied to the rotated cells also. In Fig 4(c) the vertical cell is also a normal cell that is represented in the vertical format also used to propagate the signal to other layer it can go to the main layer through vertical cells [6]. The crossover cells as shown in Fig 4(d) are used in the upper layer the signal propagates through these cells and also the calls can change the clock in the crossover, hence the delay can also be implemented in the crossover path. The QCA cells are also the memory cells which can store the value given that is the polarization, if the circuit is in need of the particular polarization, hence the Fig 4(e) the fixed polarization cells[5].

The basic logic circuits in QCA are the majority gate and the inverter. The majority gate or the majority voter gives the output that is majority in the input. The basic gate is the MV3 gate consists of three input and one output that is arranged as in the figure.Fig.5(a). The standard inverter is the 11 cell inverted that can be realized using 2 cell also as shown in the figure.Fig.5(b).



(a) (b) (c) (d) (e)

Fig. 4. Types of cells (a)normal cell (b)rotated cell (c)vertical cell (d)crossover cell (e)fixed polarized cell



(a) Majority Gate or Majority Voter with 3 inputs.

(b) Inverter Circuit

Fig. 5. Basic logic circuits in QCA.

The polarization of each cell tends to align with that of its neighbors, a linear arrangement of cells used to transmit information[7]. The continuous arrangement of the QCA cells forms the wires to propagate the signal. There are two types of the wires, the standard 90^o and standard 45^o and is achieved by placing the cells side-by-side as shown in the Fig 6(a) and 6(b)[7]. The standard 45^o is achieved by placing the rotated cells. By using the wires both co-planar crossing and multilayer crossing can be done. By placing the cell in any direction the same signal is passed and hence the crossing is used.

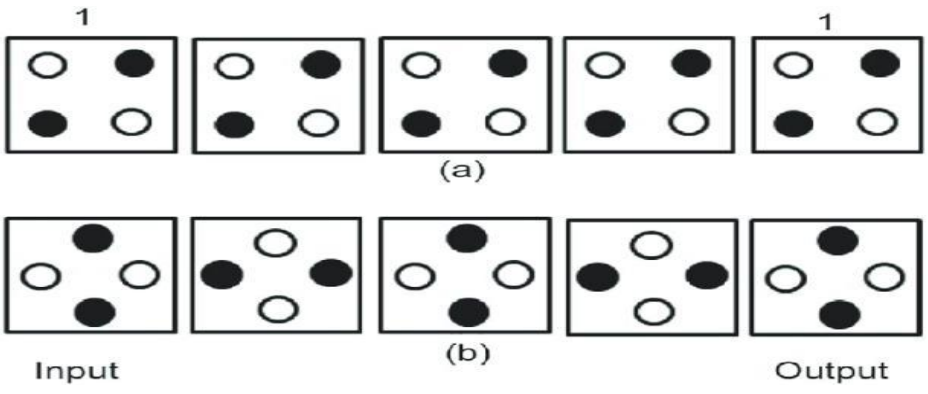


Fig.6. (a)standard 90^o wire (b)standard 45^o wire

For the single layer or coplaner crossover the crossing is implemented using both 90^o and 45^o QCA cells,These cells would pass the crossing without the effect on each other[8]. For the multilayer crossing the crossing is achieved by multilayer placement of QCA cells, both the normal cells and rotated cells can be used[9]. Also there is a crossover that is based on the clock phases called the logical wire crossing, uses one type of QCA cells and is based on the interference of clocking phases on each other and is of 180^o out of phase i.e., the phase difference must be π[10]. The tapping in QCA can be achieved by branching out the wire into multiple end-points or wire-tapping from a wire as in the conventional semiconductor technology. These end-points or taps could then serve as inputs to other gates or final output[10].

The simulation tool for the Quantum-dot cellular automata is QCADesigner, developed at the ATIPS laboratory, by Konrad Walus, University of Calgary. QCADesigner is capable of simulating complex QCA circuits and has three different simulation engines. The first is a digital logic simulator, which considers cells to be either null or fully polarized. The second is a nonlinear approximation engine, which uses the nonlinear cell-to-cell response function to iteratively determine the stable state of the cells within a design. The third uses a two-state Hamiltonian to form an approximation of the full quantum mechanical model of such a system[12]. Included in the current version of QCADesigner are two different simulation engines: the bistable and coherence vector engines[12].

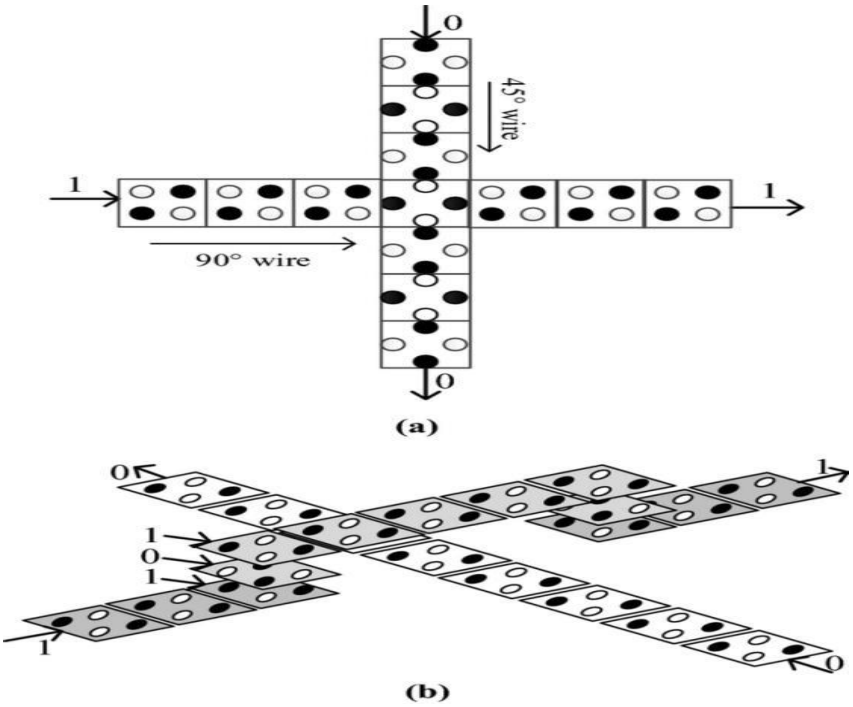


Fig.7 (a)coplanar crossover (b)multilayer crossover

2. Description

The differentiator that calculates the differentiation of the signal. For the analog signal the slope itself is the differentiation, but for the discrete signals the differentiation is the differences of the values at the moment and previous values. First-difference differentiator and Central-difference differentiator are two simple differentiators. The difference between the successive samples is the process of the First-difference differentiator. If x(n) are the input of a system then y(n) be the the first-difference derivative[1].The central difference differentiator calculates the average of difference between alternate pairs of the given sequence[1].

$$y(n) = x(n) - x(n-1) \quad (1)$$

$$y(n) = \frac{x(n) - x(n-2)}{2} \quad (2)$$

The Bilinear Transformation of the IIR filter System can be given as

$$H(s) = \frac{b}{s + a} \qquad (3)$$

This system is also characterized by the differential equation

$$\frac{dy(t)}{dt} + ay(t) = bx(t)$$

On solving the equation by using t=nT

$$y'(nT) = -ay(nT) + bx(nT)$$

For the equivalent discrete time system y(n)=y(nT) and x(n)=x(nT), we obtain

$$\left(1 + \frac{aT}{2}\right) y(n) - \left(1 - \frac{aT}{2}\right) y(n-1) = \frac{bT}{2}[x(n) + x(n+1)]$$

The z-transform of this difference equation is

$$\left(1 + \frac{aT}{2}\right) Y(z) - \left(1 - \frac{aT}{2}\right) z^{-1} Y(z) = \frac{bT}{2}(1 + z^{-1}) X(z)$$

The system function H(z) is given as

$$H(z) = \frac{b}{\frac{2}{T}\left(\frac{1 - z^{-1}}{1 + z^{-1}}\right) + a} \qquad (4)$$

The mapping from the s-plane to z-plane is

$$s = \frac{2}{T}\left(\frac{1 - z^{-1}}{1 + z^{-1}}\right)$$

This is called Bilinear transform.

$$H(z) = \frac{T}{2}\left(\frac{z - 1}{z + 1}\right) \qquad (5)$$

Equation (5) is the Integrator and the differentiator is given as the equation (6).

$$H_{diff}(z) = \frac{2}{T}\left(\frac{z - 1}{z + 1}\right) \qquad (6)$$

$$\frac{Y(z)}{X(z)} = \frac{2}{T}\left(\frac{z - 1}{z + 1}\right)$$

By taking the inverse Z transform T=1sec,

$$2[x(n) - x(n-1)] = y(n) + y(n-1)$$

$$y(n) = 2[x(n) - x(n-1)] - y(n-1) \qquad (7)$$

The digital differentiators mentioned in equations (1) and (2) are realized and the equation (7) is implemented.

Although accurate techniques for computation of derrivative of discrete-time signal are not available, there are several approximate techniques and numerical methods using which the derivative of a signal can be estimated. These techniques are used in the hardware implementation[14]. The concepts of integration and diferentiation are well defined in the analog domain since the signals are mostly continuous. Geometrically, diferentiation is the slope of a given function at the point under consideration and integration is the area under the curve of a

given function. The concept of slope and area is not clearly defned for discretetime signals, but diferentiation and integration operation play a vital role in many DSP applications[15].

To implement these differentiators we need a delay element and the subtractor. When the signal pass through the single clock zone there is no delay and the output follows till the cells are in the similar clock zone. When the clock zone changes as the phase change from one clock to the next clock is 90^o and hence the delay occurs. For a signal to have complete one bit delay, cells of all four clock zones are used side by side. Hence the delay element is formed. The delay element is as shown in the figure Fig.8.

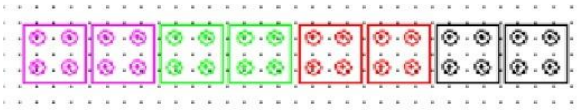


Fig.8 . Delay element

The Full subtractor is which has three inputs i.e., two inputs with borrow input, and the difference and the borrow output are the outputs. Full subtractor is implemented by using the majority gates as given in the Fig.9(a). In the similar format the the circuit is implemented in QCA layout by using the majority gates. The layout is as shown in the Fig.9(b). The X and Y are the inputs for the subtractor and for the differentiator one of the inputs is the delayed input hence the delay element is used at any of the input. This delay element used in the subtractor to delay the input bit by one cycle.

The Equation for the Difference and the Borrow when the inputs are X,Y and B_in

$$\text{Diff} = X \oplus Y \oplus B\_in$$

$$\text{Borrow} = \overline{X}Y + \overline{X}B\_in + YB\_in$$

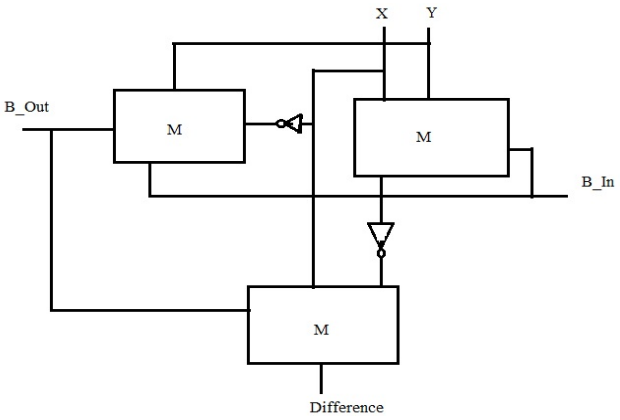


Fig. 9(a). Block diagram of Full subtractor using majority gates

Based on the Equations Full Subtractor can also be implemented using 3 input XOR gate and the Majority gate. The 2-input XOR that is implemented has the complicated circuit with the Crossovers[4]. In the [15] the 2-input and also the 3-input XOR gate is implemented without the crossovers and moving the cells. As shown in Fig.10 the Full Subtractor is implemented using the 3-input XOR gate[16].

3. Digital Differentiators

The simple differentiators used are the First difference differentiator and the Central difference differentiator. Both has the delay elements and the subtractor. This can be extended for the number of bits. In this paper the simulation is done for the four bit differentiators. For each bit, the delay element and a subtractor is placed. Here the equation (1) and equation (2) are the equations for the simple differentiators the First difference differentiator and Central Difference Differentiator. For the Central difference differentiator the division with 2 ,

the division is achieved by right shifting of a single position. The design of the simple differentiators are given below. The bilinear transformation is also a differentiator mentioned in equation (7).

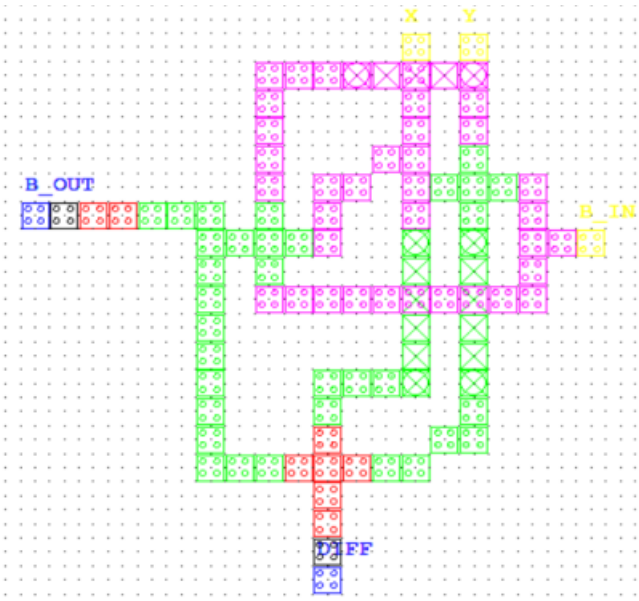


Fig. 9(b). Full subtractor QCA layout

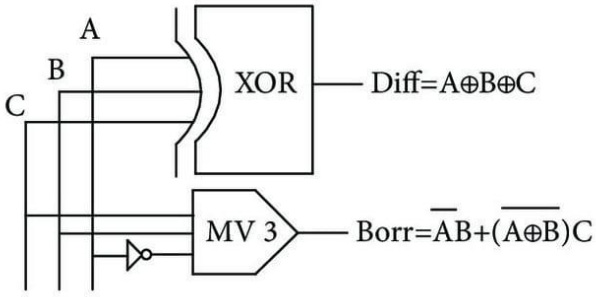


Fig.10(a) Block Diagram of Full Subtractor using 3-input Xor gate

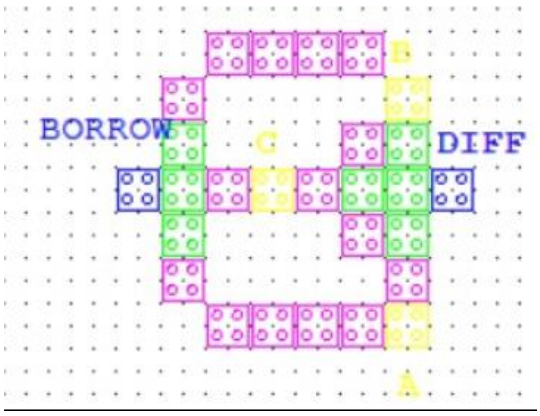


Fig.10(b) QCA Layout of Full Subtractor using 3-input xor gate

A. First Difference Differentiator

The circuit of the First difference differentiator is given in the Fig.8(a). Here in the circuit there are 4 inputs for the 4-bits also for the first subtractor there is the borrow in also be considered as input. This can also be initiated to the logic '0' that is the polarization to the level '-1' as the circuit is initially in the reset mode. At the output also the borrow out is also a output including the 4 outputs for the 4-bits, this indicates the sign of the output. To decrease the circuit complexity the subtractor used in Fig. 9 the Fig. 10 is used and the same circuit mentioned in the Fig. 11(a) is also modified using the subtractor in Fig. 10 and the resultant circuit is the circuit given in the Fig. 11(c). The corssover are used to give the borrow form one subtractor to other.

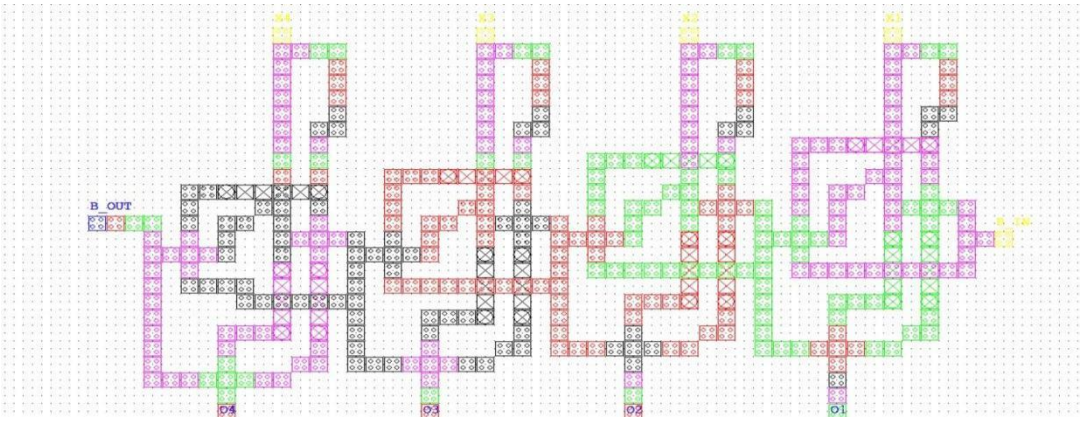


Fig. 11(a). The design of 4-bit First difference differentiator

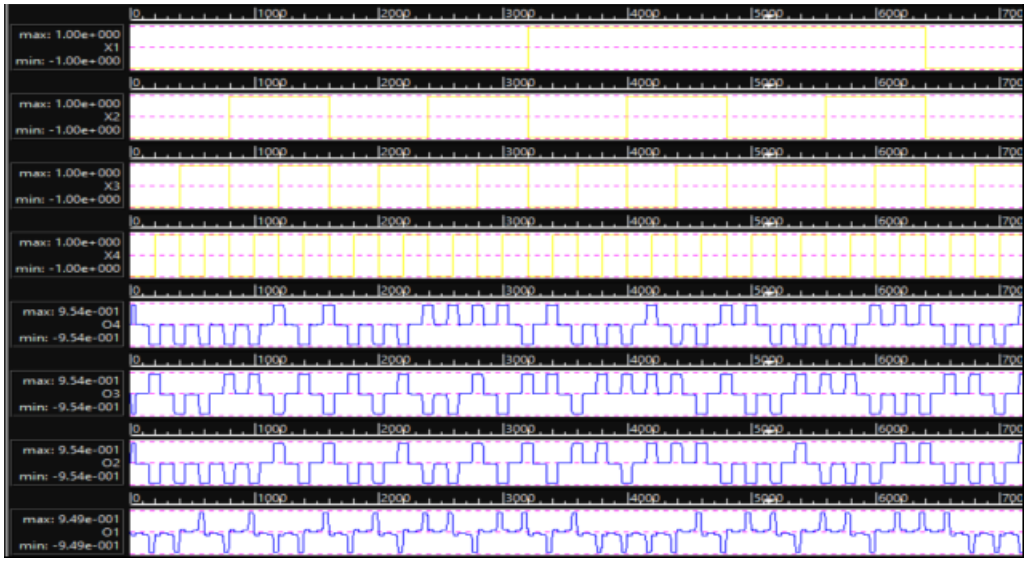


Fig. 11(b). The results of 4-bit First difference differentiator

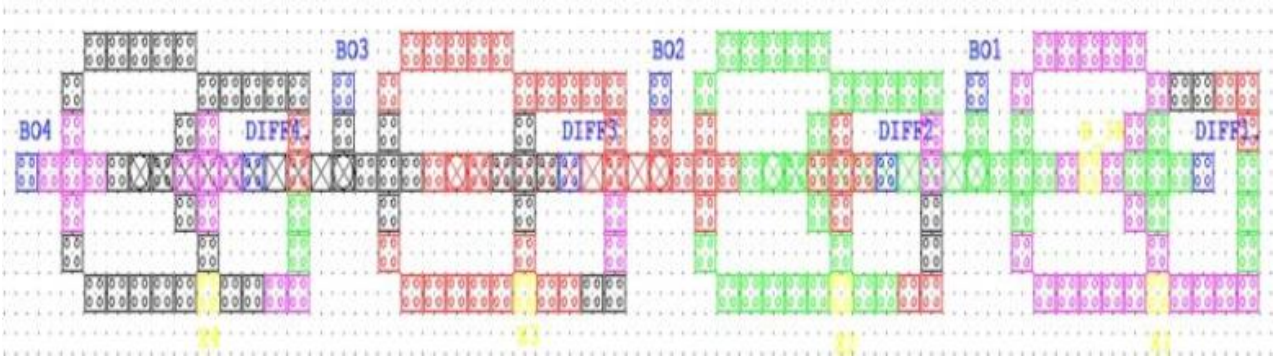


Fig. 11(c). The First Difference Differentiator with the Subtractor using the XOR gate.

Fig. 11(d). The results of First Difference Differentiator of the circuit 11(c).

B. Central Difference Differentiator

The Central difference differentiator is similar to the First difference Differentiator the delay is two times and hence the two delay elements are used in the input. The borrow is initiated to logic '0' and in the circuit the first sum is no longer used as the output is the division by 2 and hence shifted right. Hence the circuit is reduced and the MSB bit is always the logic '0' because of the shifting. The circuit of Central difference differentiator is given in the Fig.12(a). The similar logic is used and the subtractor is changed in the Fig.12(c).

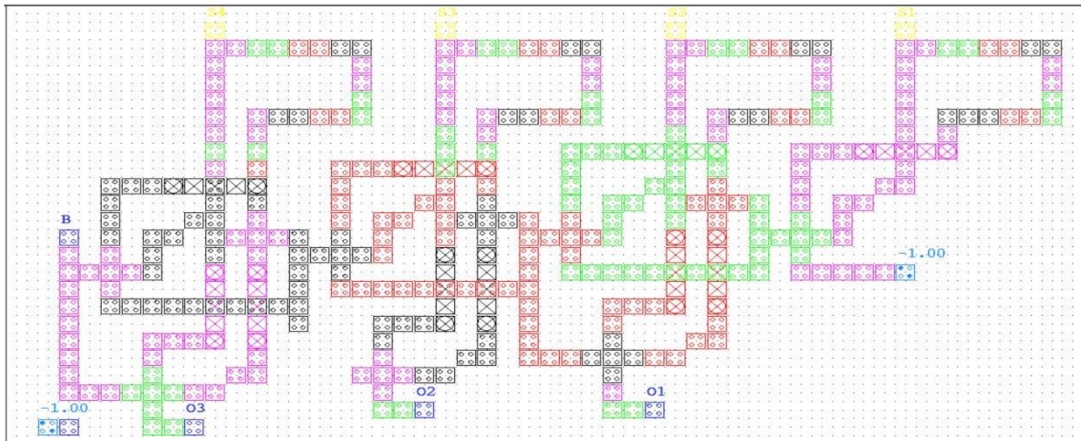


Fig. 12(a). The design of 4-bit Central difference differentiator

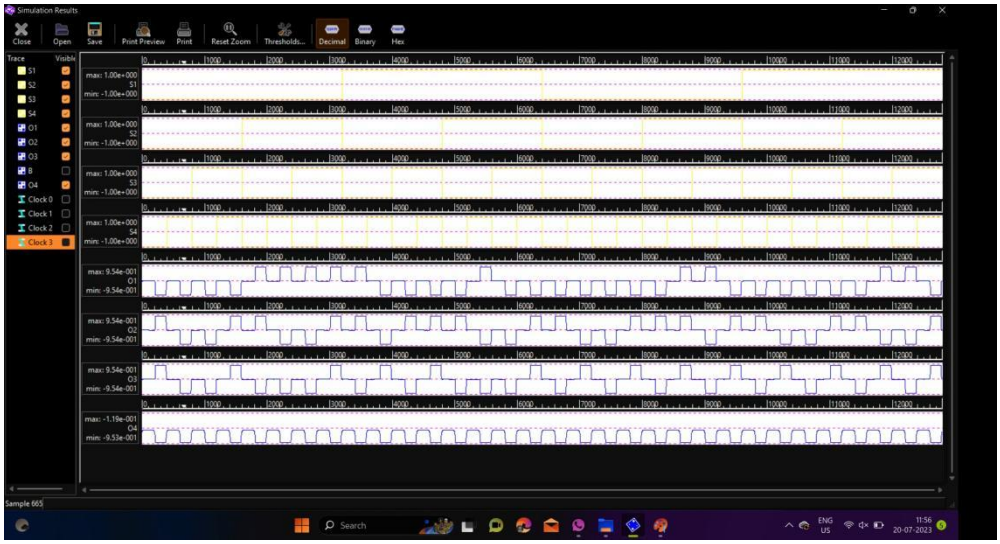


Fig. 12(b). The results of 4-bit Central difference differentiator

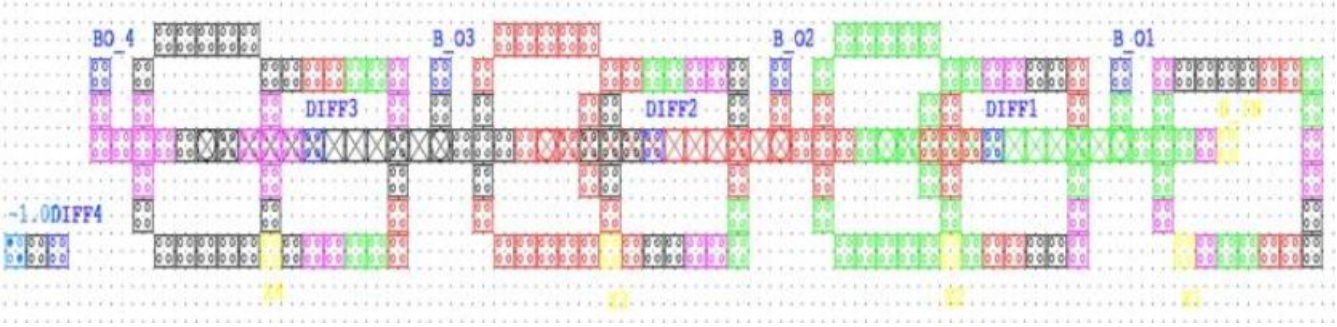


Fig. 12(c). **The Central Difference Differentiator with subtractor using XOR gate.**

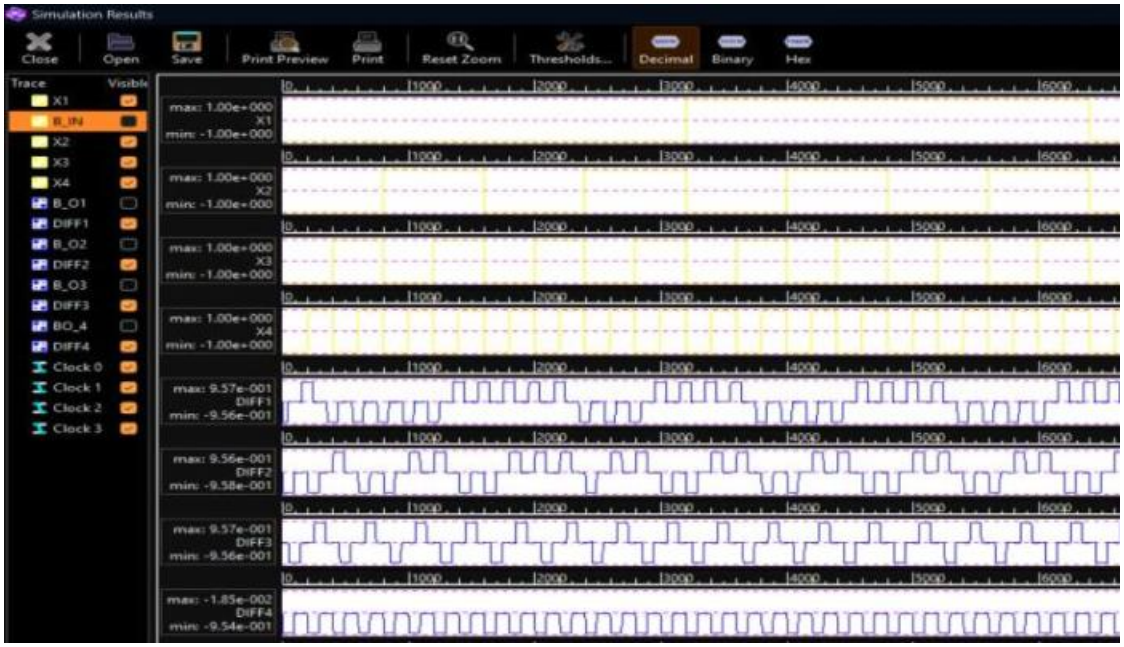


Fig. 12(d). Results of the Central Difference Differentiator for Fig.12(c)

C. Bilinear Transformation

In the Bilinear Transformation the input is subtracted by the delayed input and is multiplied by 2 as the divison is the right shift and now the multiplication is the left shift of the result hence the LSB is added with the logic zero. The result is now given to the subtractor unit and the second input to this subtractor is the delayed version of the output, the delay element is used to join the input of the subtractor and the output.

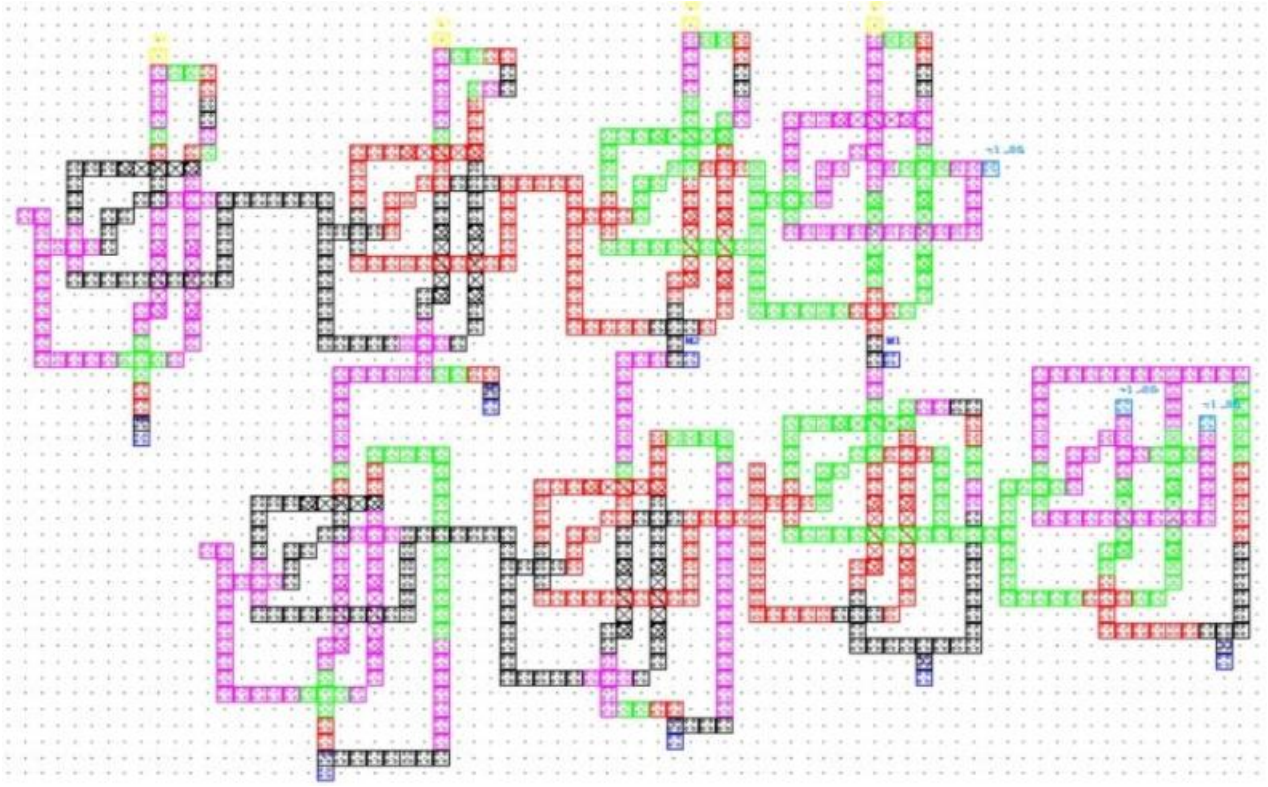


Fig. 13(a). The design of bilinear transformation

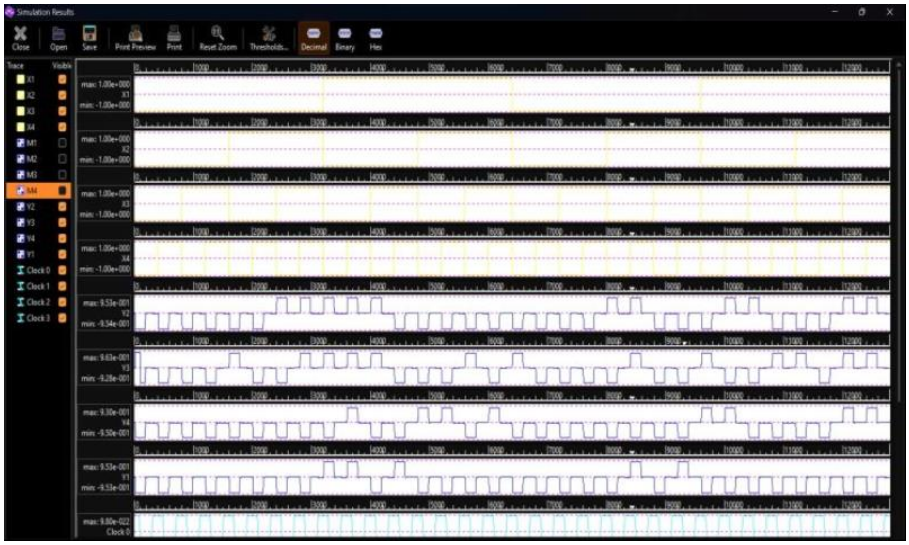


Fig. 11(b). The results of Bilinear Transformation

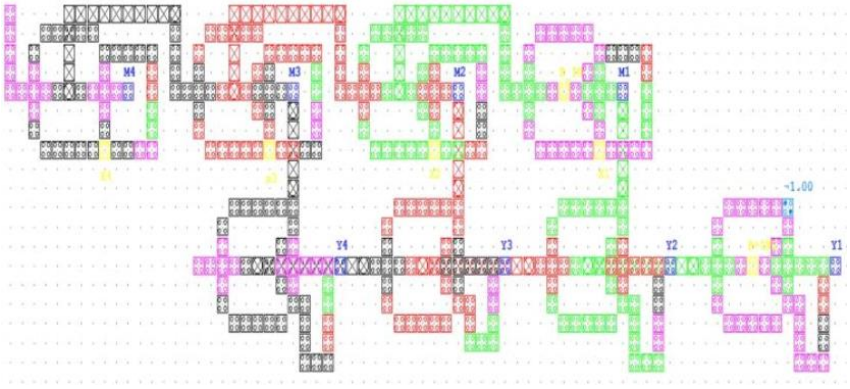


Fig. 11(c). The Bilinear Transformation with the Subtractor using the XOR gate.

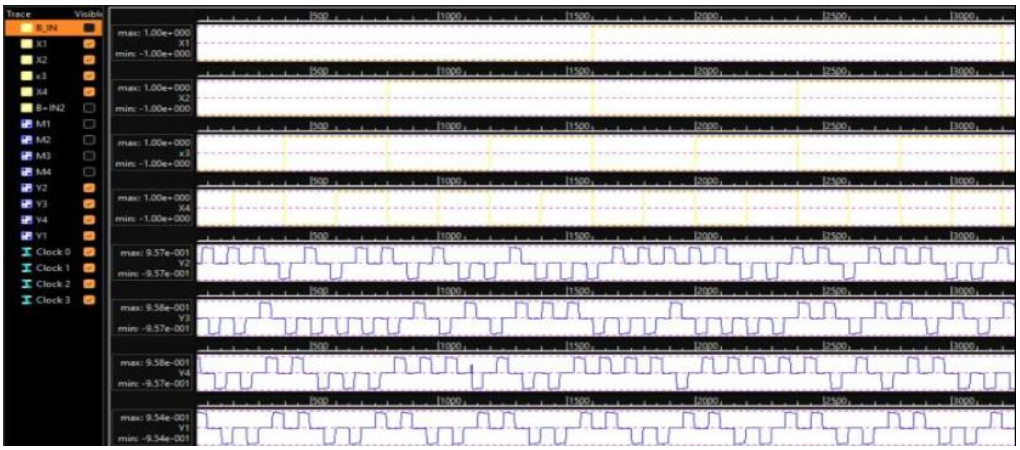


Fig. 11(d). The results of Bilinear transformation of the circuit 13(c).

4. Results and Discussions

The results of the simple differentiators are given in the Fig.11(b) and Fig.12(b) the first difference and the central difference differenetiators respectively. The input and the output cells are not in the same clock zones and also from the input to the output all the four clock zones are used, and hence there is the delay as the signal when crosses all the four clock zones there is the delay of one clock cycle. Also there is the crossover cells to avoid the disturbances and hence all the delays are considered there the output is 1.5 cycles delay from the input. More number of cells should be used to stabilize and constant output. As observed the inputs given are in the same clock that is in the clock0 and the output is taken in the same clock and is in the clock2 in Fig 11(a). It is deliberately taken as such. Whereas in the Fig.11(c) the input given in the different clocks as also the output. Similarly the input and the output of the Central Difference Differentiator and the bilinear transformation in Fig. 12(c) and Fig. 13(c) also taken in the different clocks. If the input and the outputs are taken in the bus format then all should be given in the same clock but here it given in the different clocks. For all the Fig.11(d), Fig. 12(d), Fig.13(d) the different clocks are used hence the output may not be in the synchronized pattern and hence the definite delay cannot be calculated. But each individual block cultivates the output as per the given input. Originally the circuits mentioned in Fig. 11(a) and 11(c) are same but both the outputs are not same because the inputs are not given in the same clock. Similarly for all the three differentiators both the circits that is with the conventional subtractor and the subtractor with the XOR gate are used as given in the above circuits.

5. Conclusion

Using QCA the simple digital differentiators are realized, by using the QCADesigner tool. The input and the output cells are not in the same clock zones and also from the input to the output all the four clock zones are used, and hence there is the delay as the signal when crosses all the four clock zones there is the delay of one clock cycle. Also there is the crossover cells to avoid the disturbances and hence all the delays are considered there the output is 1.5 cycles delay from the input. The clocking concept become the main challenge in the physical design of circuit in QCA, is observed when the increase of the circuit complexity in last number of timing waveform obtained will add more delay. The area is reduced from the circuit implemented with default subtractor to the circuit implemented with the XOR gate. With that the simulation speed is also increased as number of cells are reduced as compared the both circuits.

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