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A Three-phase Thirteen-level Voltage Source Inverter with Inherent Gain

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Abstract

Switched Capacitor Multilevel Inverters (SCMLIs) provide advantages such as integrated voltage boosting capability; and easy voltage balancing of capacitors. However, many existing SCMLI designs are primarily intended for single-phase applications, necessitating three separate DC sources for three-phase applications. This work introduces a novel SCMLI capable of generating seven voltage levels at each pole, including positive, negative, and zero levels, and thirteen levels in the line voltage. Significantly, the proposed inverter requires only a single input DC source for three-phase operation. In order to validate the proposed SCMLI topology, both simulation and experimental results are presented.

Keywords: Multilevel inverter; Switched capacitors; Voltage boosting; Self balanced capacitors

1. Background

Since their origin in the 1970s, multilevel inverters (MLIs) are being used in areas which require high quality DC-to-AC conversion, such as: adjustable speed drives, photovoltaic power generation systems, electric vehicles etc. [1-3]. Stepped waveform synthesized by MLIs exhibit much better harmonic profile as against the two-level inverters, thereby greatly reducing the filtering requirements. In addition, the dv/dt stress imposed by a multilevel AC waveform is much lower than a 2-level waveform. MLI linkage structure generally permit low-voltage power switch use. These advantages are also propelling the diversification of MLIs to applications such as high-power-density apparatus [4], contactless power transfer [5] and high voltage DC transmission [6]. These applications, however, are mainly dominated by the conventional topologies of MLIs, viz. diode-clamped, cascaded H-bridge, flying capacitors, modular multilevel converters, as well as active neutral point clamped topologies [7]. These topologies typically necessitate an increased quantity of devices when synthesizing a waveform with several levels. Additionally, these conventional MLIs exhibit a unity voltage-gain, with no inherent voltage boosting. Such inherent voltage boosting is of great importance in applications where the input DC power sources of low-voltage are involved. Photovoltaic panels used in renewable systems are such example[8]. This has led to an evolution of a novel category of MLIs, known as 'switched capacitors based multilevel inverters' or 'SCMLIs' [9]. In these topologies, the switched capacitors (SCs) principle is employed wherein certain switching combination(s) are such that input DC source are in parallel with capacitor, thereby charging it approximately to the input source voltage. Thereafter, when connected to the load during other switching combination(s), capacitor and DC source series combination has been there. With such mechanism, the switched capacitors not only step-up the voltage, but they also add levels to the output multilevel waveform. Self-balancing these capacitors has been another significant SCMLIs application because it greatly reduces the requirement of additional circuitry for voltage regulation (moreover a intricate control methodology thereof).

In view of the aforementioned advantages of SCMLIs, numerous novel topologies have been proposed [8]. These works, however, are mainly focused on the development of single-phase SCMLI structures. The SCMLI proposed in [10] aims at reduction of device count and total-blocking-voltage, but requires numerous DC sources which have been needed as electrically isolated. SCMLI voltage gain presented in [11] is very high, but it requires high

voltage power switches. The SCMLI proposed in [12] has a high component count. Many of the recently proposed SCMLI structures use multilevel switched capacitors based DC-to-DC conversion stage as the front end and thereafter an H-bridge is connected so as to synthesize a bipolar multilevel waveform. Topologies presented in [12-14] are examples of such structures with generalized formulations. The SCMLI topologies proposed in [15] and [16] use voltage doubling based on the SC principle as the front end, in conjunction with an H-bridge, whereas an SC based voltage tripling unit is utilized in the topology proposed in [17]. Other approaches to synthesize SC based stepped-up voltages as inputs to H-bridge are proposed in [18] and [19], wherein respective front-ends employ cross-switched and bridge modular units. A few topologies, such as those discussed in [20-23], use two half-bridges with SC-based unit inserted in-between. In H-bridge configuration, all 4switches of H-bridge must withstand for blocking one voltage identical to output AC multilevel waveform's peak value, while only two switches experience such large voltages in the latter approach involving two half-bridges. In both these approaches, however, extension of these topologies to their respective three-phase version is extremely difficult [24]. Such direct extension to three-phase would require electrically isolated input DC sources for each leg; moreover quantity of power switches would be significantly high. Even when these topologies are reconstructed with for three-phase application, it would entail a development of new modulation schemes, analysis and design approach [24].

In the research work presented here, a new SCMLI has been conceptualized which can synthesize three-phase stepped-up AC voltages using only one input SC source. The output AC voltage waveform comprises 7levels in all phases & 13 levels in the line voltages. Since the switched capacitors principle is employed, all the capacitors are automatically balanced, without requiring sensors for this purpose. The proposed topology offer both phase- as well as line-redundancies using which a comprehensive fault-tolerant operation can be realized. The topology and it's working described in section II. A modulation procedure has been described in section III, while design parameters are discussed in section IV. Simulation and experimental outputs of proposed inverter have been stated in section V. Also, in section VI, suggested topology has been compared to other SCMLIs. Conclusion is given in section VII.

2. Details of the Proposed Multilevel Inverter

2.1. Power Circuit

The proposed SCMLI topology offers a novel design for converting low DC voltages into high-quality three-phase AC outputs. The topology consists of three legs indicating the three phases each. All three phases are powered by a common DC voltage source (V_{dc}), as shown as in Fig. 1, with two DC link capacitors (C_1, C_2) each having a voltage of $0.5V_{dc}$. Each leg of the proposed inverter uses two capacitors, eight active power switches along with 2 diodes.

Power switches S_1, S_2, S_3 and S_4 for each leg are labelled according to the leg (please refer to Fig. 1). Similarly, switches $\overline{S_1}$, $\overline{S_2}$, $\overline{S_3}$ and $\overline{S_4}$ are complentary respectively to S_1, S_2, S_3 and S_4. So, if "1" refers to "ON" state of a switch & "0" refers to its "OFF" state, then:

$$\overline{S_{a1}} = 1 - S_{a1} \quad (1)$$

$$\overline{S_{a2}} = 1 - S_{a2} \quad (2)$$

$$\overline{S_{a3}} = 1 - S_{a3} \quad (3)$$

$$\overline{S_{a4}} = 1 - S_{a4} \quad (4)$$

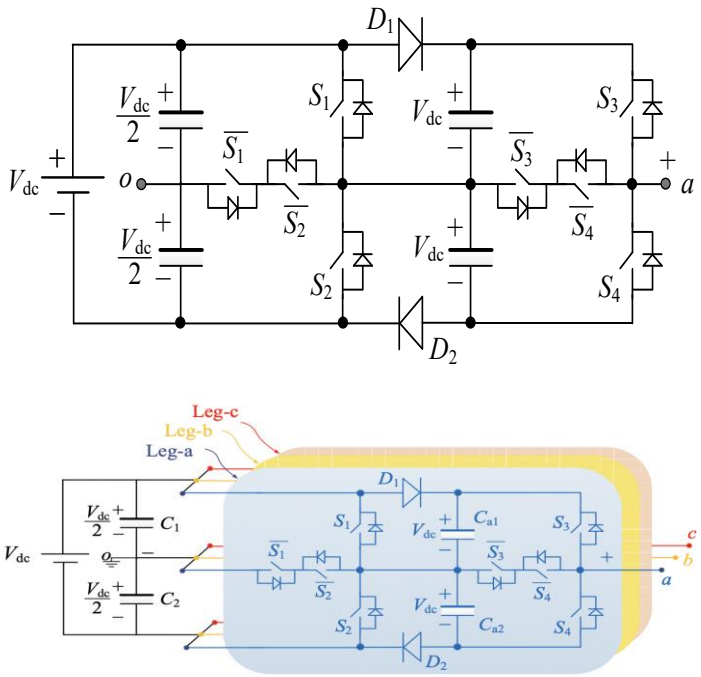


Fig. 1 (a) One leg of the SCMLI proposed in this work (b) The three-phase configuration of the proposed topology.

Capacitors in legs are balanced at a voltage of V_{dc}. The pole voltages (V_{xo}) {where $x \in a, b, c$}, thus, have seven voltage levels: $\pm 1.5V_{dc}$, $\pm V_{dc}$, $\pm 0.5V_{dc}$ and 0. For a given leg 'a', the pole voltage V_{ao} can be expressed as:

$$V_{ao} = V_{dc}[0.5(S_{a1} - S_{a2}) + (S_{a3} - S_{a4})] \tag{5}$$

Other pole voltages follow similar expressions. Also, the expressions for line voltages would be:

$$V_{ab} = V_{ao} - V_{bo} \tag{6}$$

$$V_{bc} = V_{bo} - V_{co} \tag{7}$$

$$V_{ca} = V_{co} - V_{ao} \tag{8}$$

2.2. Description of switching states for one leg of the proposed SCMLI

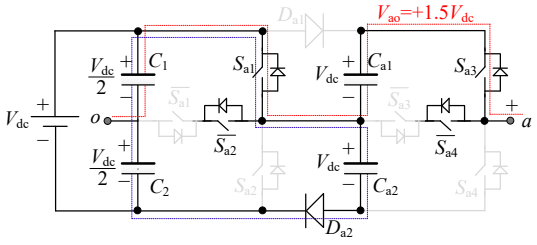
In Table 1, the valid switching states for leg 'a' of the inverter shown in Fig. 1 are summarized, wherein "1" and "0" respectively refer to ON and OFF conditions of a given power switch.

Table 1. Operating States for leg 'a' of the proposed inverter

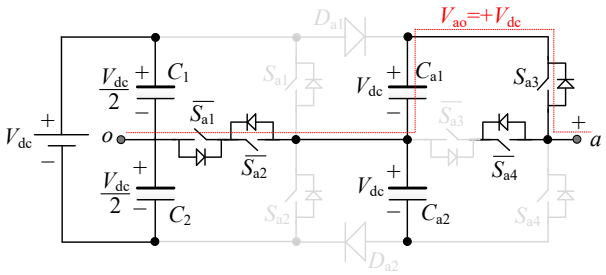
States	Switch State				Capacitor State		$V_{ao}=V_{dc}[0.5(S_{a1}-S_{a2})+(S_{a3}-S_{a4})]$
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	C_{a1}	C_{a2}	
λ_{a1}	1	0	1	0	D	C	$+1.5V_{dc}$
λ_{a2}	0	0	1	0	D	N	$+V_{dc}$
λ_{a3}	0	1	1	0	C	N	$+0.5V_{dc}$
λ_{a4}	0	0	0	0	N	N	0
λ_{a5}	1	0	0	1	N	C	$-0.5V_{dc}$
λ_{a6}	0	0	0	1	N	D	$-V_{dc}$
λ_{a7}	0	1	0	1	C	D	$-1.5V_{dc}$

Also, in Table 1, letters "C", "D" and "N" are respectively employed to indicate discharging, charging, and 'no-change' states of the capacitors. It must be noted that the working states of the other legs would be similar. These switching states are briefly discussed below.

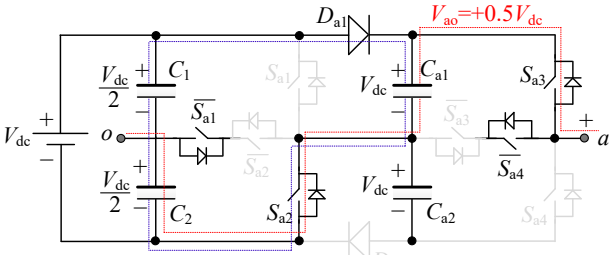
- **State λ_{a1} ($V_{ao}=+1.5V_{dc}$):** In this state, the switches which are simultaneously turned ON are $S_{a1}, S_{a3}, \overline{S_{a2}}$ and $\overline{S_{a4}}$, thereby synthesizing a pole voltage equal to $+1.5V_{dc}$. In this state, the capacitor C_{a2} gets charged through DC link capacitors and the capacitor C_{a1} gets discharged to load as can be seen in Fig. 2(a).
- **State λ_{a2} ($V_{ao}=+V_{dc}$):** When power switches $\overline{S_{a1}}, \overline{S_{a2}}, S_{a3}$ & $\overline{S_{a4}}$ are simultaneously switched ON, a pole voltage equal to $+V_{dc}$ is synthesized. In this state, the capacitor C_{a1} gets discharged to the load and the capacitor C_{a2} is bypassed (i.e. does not undergo any change) as illustrated in Fig. 2(b).
- **State λ_{a3} ($V_{ao}=+0.5V_{dc}$):** For this state, power switches $S_{a2}, S_{a3}, \overline{S_{a1}}$, & $\overline{S_{a4}}$ have been simultaneously switched ON, thereby synthesizing a pole voltage equal to $+0.5V_{dc}$. During this state, the switched capacitor C_{a1} is charged through capacitors C_1 and C_2. Also, during this state, the capacitor C_{a2} is bypassed (i.e. it does not undergo any change) as can be seen in Fig. 2(c).
- **State λ_{a4} ($V_{ao}=0$):** On simultaneously turning ON power switches $\overline{S_{a1}}, \overline{S_{a2}}, \overline{S_{a3}}$ & $\overline{S_{a4}}$, a pole voltage equal to zero is synthesized. In this state, both the capacitors C_{a1} and C_{a2} are bypassed as state shown in Fig. 2(d).
- **State λ_{a5} ($V_{ao}=-0.5V_{dc}$):** On simultaneously turning ON power switches $S_{a1}, S_{a4}, \overline{S_{a2}}$, & $\overline{S_{a3}}$, a pole voltage equal to $-0.5V_{dc}$ is synthesized. During this switching combination, the capacitor Ca2 gets charged through the capacitors C1 and C2, while the capacitor Ca1 is bypassed, as shown in Fig. 2(e).
- **State λ_{a6} ($V_{ao}=-V_{dc}$):** On simultaneously turning ON power switches $\overline{S_{a1}}, \overline{S_{a2}}, \overline{S_{a3}}$ & S_{a4}, a pole voltage equal to $-V_{dc}$ is synthesized. In this state, the capacitor C_{a2} gets discharged to the load and the capacitor C_{a1} is bypassed, as neutral in this state shown in Fig. 2(f).
- **State λ_{a7} ($V_{ao}=-1.5V_{dc}$):** On simultaneously turning ON power switches $\overline{S_{a1}}, S_{a4}, \overline{S_{a3}}$ & S_{a4} , a pole voltage equal to $-1.5V_{dc}$ is synthesized. For this switching combination, the capacitor C_{a1} gets charged through the capacitors C_1 & C_2, and capacitor C_{a2} is connected to the load, thereby getting discharged, as shown in Fig. 2(g).

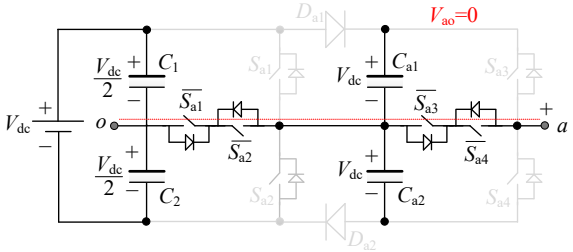


(a) V_{ao}= +1.5V_{dc}



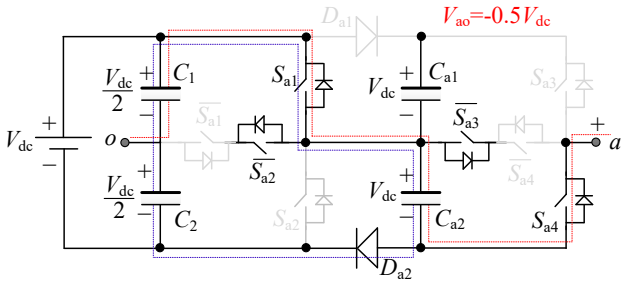
(b) V_{ao}=+V_{dc}

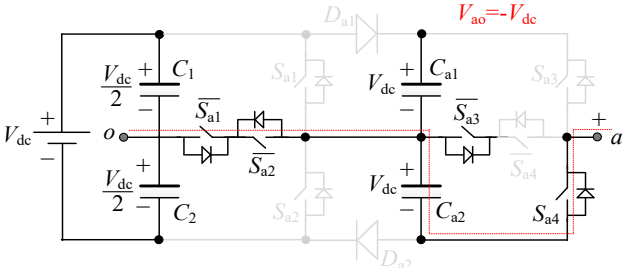




(c) V_{ao}= +0.5V_{dc}

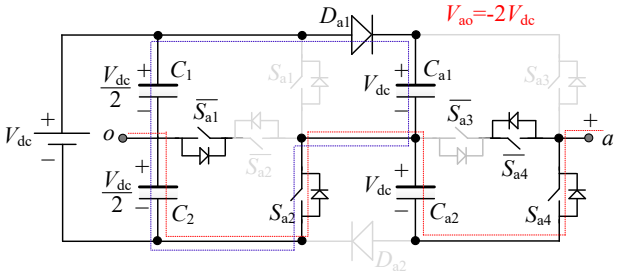
(d) V_{ao}= 0





(e) V_{ao}= -0.5V_{dc}

(f) V_{ao}= -V_{dc}



(g) V_{ao}= -1.5V_{dc}

Fig. 2 Conduction paths for various switching states pertaining to one leg of the proposed inverter with pole voltage values as: (a) Vao= +1.5Vdc, (b) Vao= +Vdc,(c) Vao= +0.5Vdc,(d) Vao= 0,(e) Vao= -0.5Vdc,(f) Vao= -Vdc,(g) Vao= -1.5Vdc

2.3. Peak-inverse-voltage (PIV) of various power switches

For each leg of the inverter proposed in this work, the peak-inverse-voltage (PIV) values for various power switches range from 0.5V_{dc} to 2V_{dc}, with V_{dc} being the input voltage and 3V_{dc} being the peak value of the output line voltage. These values are summarized in Table 2.

Table 2. PIVs values of various power switches in one leg of the proposed SCMLI

PIV	Power switches
0.5 V_{dc}	$\overline{S_1}$, $\overline{S_2}$
V_{dc}	D_1, D_2, S_1, S_2, $\overline{S_3}$, $\overline{S_4}$
2V_{dc}	S_3, S_4

2.4. Capacitance calculations

In the proposed inverter, the two DC-link capacitors (viz. C_1 and C_2) are connected directly with the input DC source (essentially acting like voltage divider) and thus, they are maintained at the desired voltage level equal to 0.5V_{dc}. The switched capacitors C_{a1} and C_{a2}, on the other hand, are to be maintained at a voltage level of V_{dc} each using the switched capacitors principle. These capacitors undergo discharge when they are connected to the load. Such discharge causes ripples in the voltage across these capacitors. Generally, voltage ripples across these capacitors should be within 10% of the voltage at which they are to be balanced. Voltage ripple across a capacitor depends on its capacitance, the discharging current (i.e. the load current) and the duration for which discharging takes place. Now, if the load is of purely resistive nature, then it is considered as the worst case leading to capacitor discharge. As seen from Fig. 2, the switched capacitor C_{a1} undergoes discharge without any in-between charging state when the transitions take place between the pole voltage levels V_{dc} and 1.5V_{dc}. Similarly, the capacitor C_{a2} undergoes discharge without any in-between charging state when the transitions take place between voltage levels -V_{dc} and -1.5V_{dc} in the pole voltage. Thus, with reference to Fig. 3, the maximum discharge in C_{a1} takes place during the angular span shown therein.

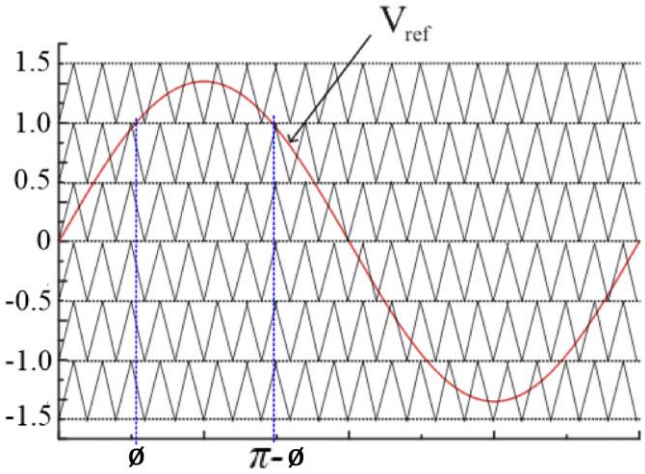


Fig. 3 Waveforms for carrier and reference for the modulation of each leg of the proposed SCMLI

Consequently, if the amplitude modulation index is 'm' and the power frequency in radian per second is $\omega_o=2\pi f_{ref}$, then for a resistive load (R_L), the discharge (ΔQ_{Ca1}) would be derived as:

$$1.5 * m * sin\text{ø} = 1 \tag{9}$$

$$\text{ø} = sin^{-1}\frac{2}{3*m} \tag{10}$$

$$\Delta Q_{Ca1} = \int_{\frac{\text{ø}}{\omega_o}}^{\frac{\pi-\text{ø}}{\omega_o}} \frac{1.5*V_{dc}}{R_L} dt \tag{11}$$

Assuming a limit of 10% voltage ripples on the capacitor,

$$100 * \frac{\Delta V_{Ca1}}{V_{dc}} \leq 10 \tag{12}$$

$$C_{a1} \geq \frac{1.5}{\omega_o * R_L}\left\{\pi - 2 * sin^{-1}\left(\frac{2}{3*m}\right)\right\} \tag{13}$$

$$C_{a1} = C_{a2} \tag{14}$$

3. Comparison with other topologies

As previously discussed, this inverter's boosting feature allows it to synthesize a high voltage AC waveform from a low voltage input DC. Conventional MLIs (such as diode clamped and flying capacitors topologies) lack this feature. As a result, a fair comparison between the suggested inverter and the conventional four-level MLIs is very challenging. This section still makes an effort to contrast their benefits and differences. In case of designing a motor driver for all topologies of inverter it is seen that the boosting factor of 0.5 is shared by the neutral point clamped and flying capacitors multilevel topologies. Same is the case with the topologies derived from the conventional ones, such as the 'nested neutral point' topology [25], the 'hybrid-clamped' topology [26], and the 'active neutral point clamped' topology [27], [28]. For the topology proposed in this work, the input DC voltage

is lower because of its higher boosting factor of 1.5. The three-phase version of the proposed inverter has twenty-four power switches, six diodes and six capacitors, and it produces a seven-level waveform (in the pole voltage), exhibiting a much higher quality output voltage and reduced dv/dt stress than the four-level output inverters.

A brief comparison can also be made with the SC-based boost inverter discussed in [29]. To obtain the appropriate line voltages, the voltage of the DC for the topology in [29] is higher, and its input DC voltage is also higher as compared to the suggested topology where the input voltage requirement is lower because of its higher boosting capability.

SCMLIs are evaluated mainly by using 'cost-function' (CF) [18,24], expressed as:

$$CF = \left(\frac{N_{IS}}{N_L}\right) * \left\{N_S + N_D + N_{AD} + N_{GD} + N_C + \left(\frac{\alpha * TSV}{\beta}\right)\right\} \quad (15)$$

where,
N_{IS} = number of DC sources used as input for the given SCMLI;
N_L = number of voltage levels in the waveform of the line voltage;
N_S = number of controlled power switches (transistors) in the given SCMLI;
N_D = number of diodes which are in anti-parallel with the main power switches;
N_{AD} = number of other diodes in the power circuit;
N_{GD} = number of driving units for the gates of the controlled switches in the given SCMLI;
N_C = total number of capacitors in the given SCMLI;
TSV = total standing voltage (in terms of the value of the input voltage);
β = inherent boosting factor (or gain); and
α = a weightage assigned to the TSV.
It has been determined that the SCMLI topology proposed in this work has a significantly low value of CF (viz. 7.308).

4. Simulation and Experimental Results

The proposed SCMLI has been simulated using MATLAB/Simulink and the simulation results are presented in this section. A description of various parameters used both for simulation and experimentation is given in Table 3.

Table 3. Various parameters pertaining to simulation and experimental studies on the proposed SCMLI

Parameter	Value	Unit
DC Source	100	V
Capacitance (C_1, C_2, C_{a1}, C_{a2})	12	mF
Power frequency	50	Hz
Carrier frequency (f_{SW})	10	kHz
Modulation depth (m)	0.95	-
Resistive-Inductive Load (3-∅ star connected)	50, 120	Ω, mH

The simulation results for the proposed three-phase SCMLI loaded with star connected balanced load of 50Ω-120 mH are shown in the following figures. In Fig. 4, the three pole voltages, along with the output currents are shown.

In Fig. 5, the line voltages waveforms of the presented topology are shown. In Fig. 6, the voltage waveforms across various power switches of one leg of the designed topology have been shown. The voltage waveforms across C_1, C_2, C_{a1}, C_{a2} of one leg of the proposed topology are shown in Fig. 7. It is clearly seen that for an input voltage of 100V, the proposed SCMLI can synthesize thirteen levels in the line voltage with a peak value of 300V.

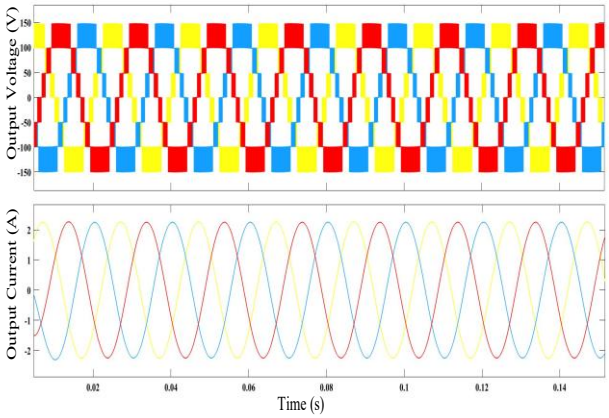
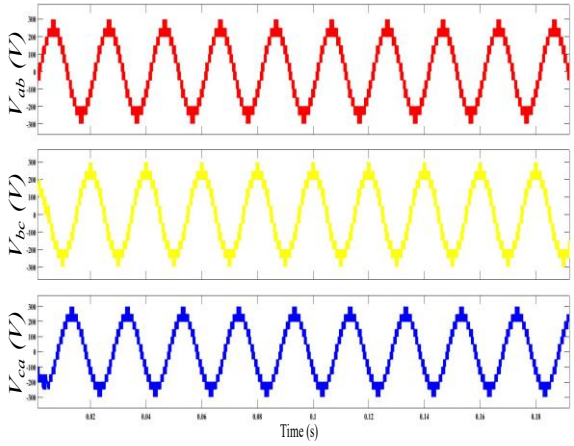


Fig. 4 Waveforms for pole voltages and output currents for the proposed topology

a



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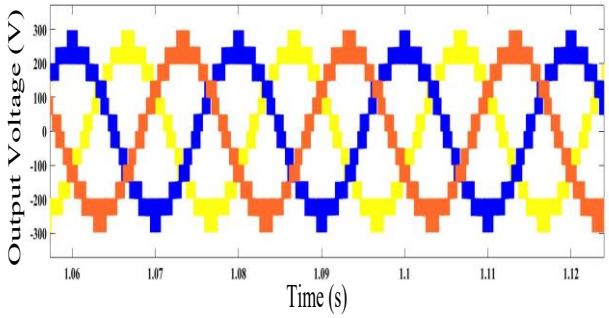

Fig. 5 Waveforms for the line voltages pertaining to the proposed SCMLI

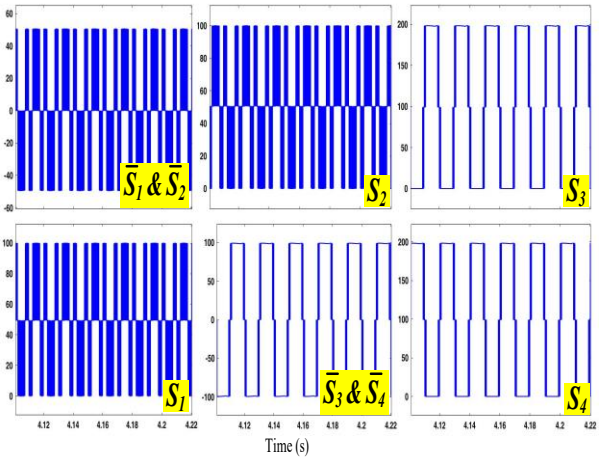

Fig. 6 Voltage waveforms across various power switches of one leg

A laboratory scale set-up of the proposed SCMLI was developed for experimental validation. The set-up uses an input DC voltage of 100V obtained from a regulated power supply of the make of Magna Power. Various parameters used for running the set-up are shown in Table 3. A photograph of this set-up is shown in Fig. 8. In order to obtain the real-time gate pulses, OPAL-RT (OP4510) real-time controller is employed, which has been interfaced with MATLAB/Simulink. Fig. 9 shows the line voltages of legs 'a', 'b', and 'c'. The three output currents are shown in Fig. 10**.** Fig. 11 represents the voltages across the power switches of one leg of the designed topology. Fig. 12 represents the voltages across the capacitors C_1, C_2, C_{a1}, C_{a2} of one leg of the proposed topology. Fig. 13 represents the pole voltage and output current of the leg 'a' of the proposed topology

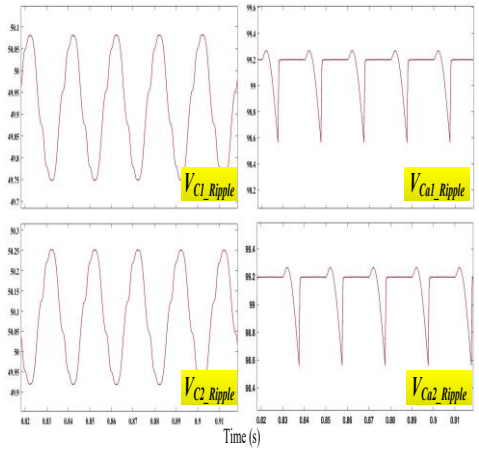

Fig. 7 Voltage waveforms across the capacitors of one leg of the proposed topology

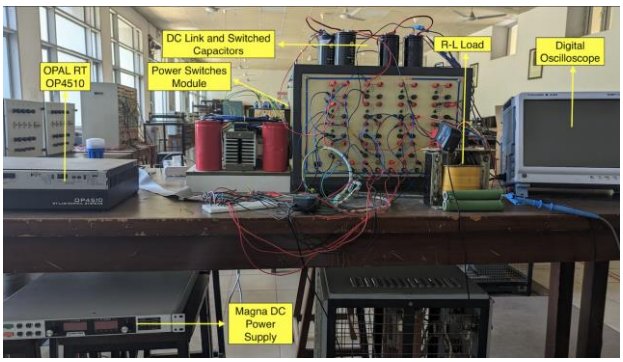

Fig. 8. Labelled picture of the experimental set-up for the proposed SCMLI

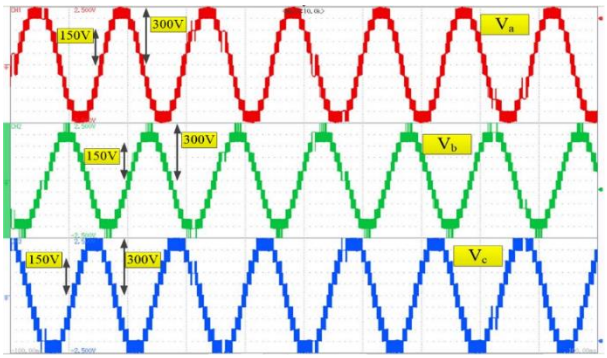

Fig. 9 Output line voltage waveforms of legs 'a', 'b', 'c'

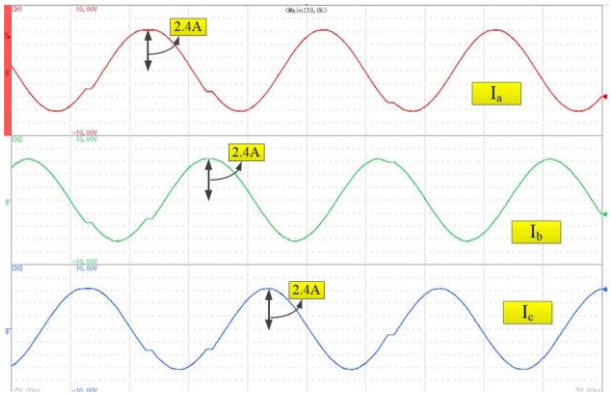

Fig. 10 Output currents for the three legs

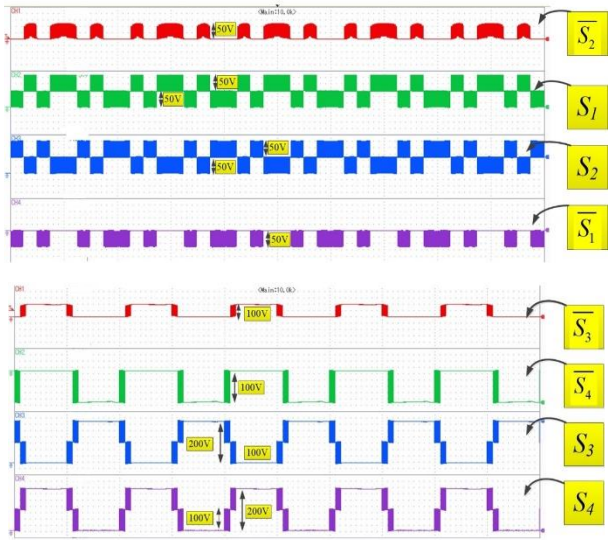

Fig. 11 Voltage waveforms across power switches of one leg

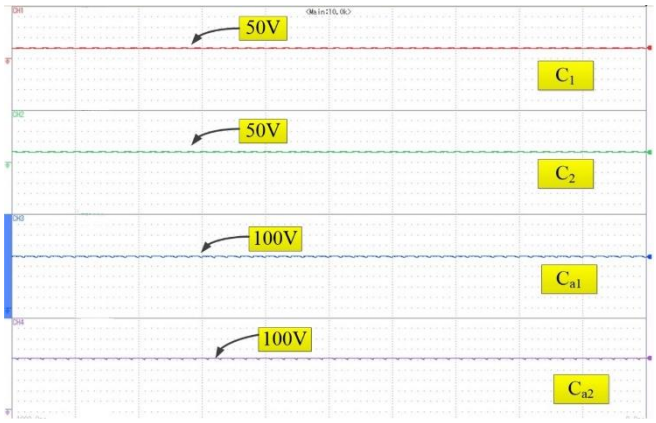

Fig. 12. Voltage waveforms across capacitors C_1, C_2, C_{a1}, and C_{a2} of leg '*a*'

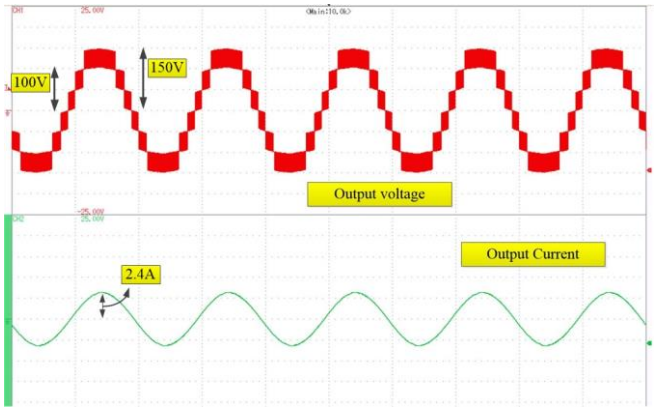

Fig. 13. Waveforms for the output pole voltage and current of leg '*a*'

5. Conclusion

This work presents a new multilevel inverter topology based on switched capacitors, designed to convert low DC voltage from a single source into three-phase stepped-up AC voltages. The topology synthesizes seven levels in each phase, and thirteen levels in the line voltages. The SCMLI's inherent self-balancing capacitors ensure system stability, while its bipolar levels in the pole voltage offer phase- and line redundancies, facilitating comprehensive fault-tolerant operation. These attributes make the proposed SCMLI a promising solution for various applications requiring high-quality AC power generation, such as renewable energy systems.

Conflicts of Interest

The authors declare that there is no conflict of interest regarding the publication of this paper.

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